Analog Reinvented

ES9039Q2M

32-bit High Performance 2 Channel DAC

Product Datasheet

The ESS SABRE® ES9039Q2M is a high performance 32-bit, 2-channel audio D/A converter. It has been designed for professional applications (mixer consoles, digital audio workstations), audiophiles-grade portable applications (headphones, network streamers and digital music players), and consumer applications (DACs and A/V receivers). The ES9039Q2M uses the newest ESS patented Hyperstream® IV Dual DAC™ technology, and advanced SABRE HiFi® architecture.

The ES9039Q2M delivers a performance level that will satisfy the most demanding audiophile and pro-audio enthusiast.

The ES9039Q2M SABRE® DAC improves on previous designs to include:

- TDM & SPI support for more options in connectivity
- Lower power consumption than previous generations which includes the Hyperstream IV DAC modulator
- New hardware mode (HW) programmability alleviates I²C/SPI programming for ease of use

The versatile audio input port accepts PCM (TDM/LJ/RJ/I²S), DSD, DoP, and S/PDIF formats. The integrates SABRE® DAC supports up to 32-bit 768kHz PCM & DSD1024 audio data via master/slave interface in synchronous and asynchronous sampling modes.

The integrated digital regulator reduces PCB area and BOM cost.

FEATURE	DESCRIPTION
Patented 32-bit Hyperstream® IV Architecture and Dual DAC™ Technology	32-bit audio DAC with very high dynamic range & ultra-low distortion
+130dB Dynamic Range (DNR) -126dB Total Harmonic Distortion (THD) -120dB Total Harmonic Distortion + Noise (THD+N)	High performance 32-bit audio DAC with unprecedented dynamic range and ultra-low distortion. Supports synchronous and asynchronous sampling modes
Integrated low noise digital regulator	Reduced BOM cost and improved DNR
32-bit processing	Distortion free signal processing
Versatile digital audio input port	Supports master/slave PCM (TDM, I²S, LJ, RJ), DSD, DoP, S/PDIF formats.
Customizable digital filter characteristics	8 preset filters and a programmable filter for custom sound signature
FIR & IIR filter bypass	To allow full customer ability to add custom filters

APPLICATIONS

- Professional digital audio workstations and mixer consoles
- Digital music players, Portable multimedia players
- Consumer and Audiophile DAC headphone amplifiers and A/V receivers
- Bluetooth stereo devices & Networked audio
- DJ equipment

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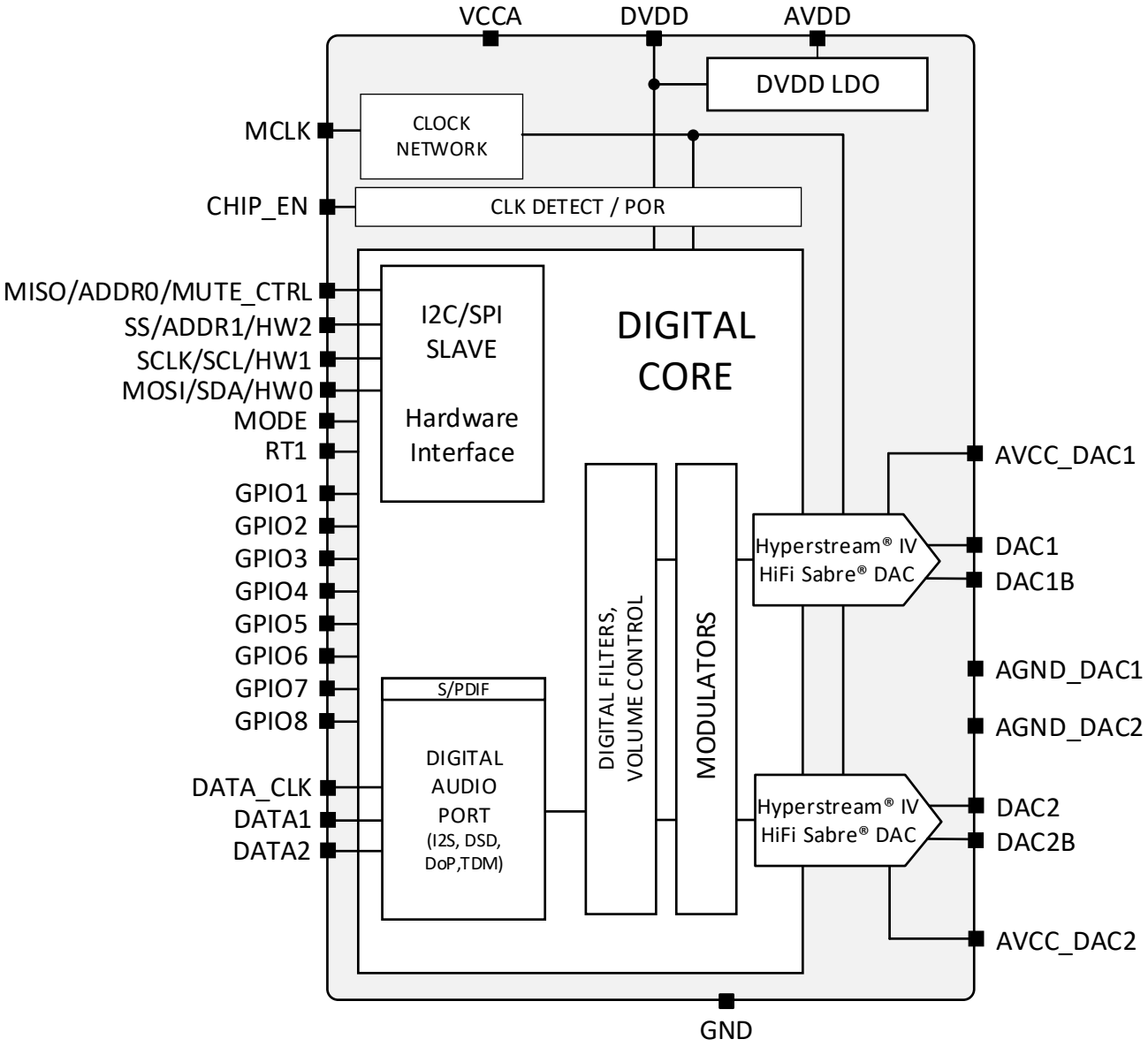


Figure 1 - Functional Block Diagram

ES9039Q2M Package

32 QFN Pinout

(Pin 33 is QFN package pad, see package dimensions)

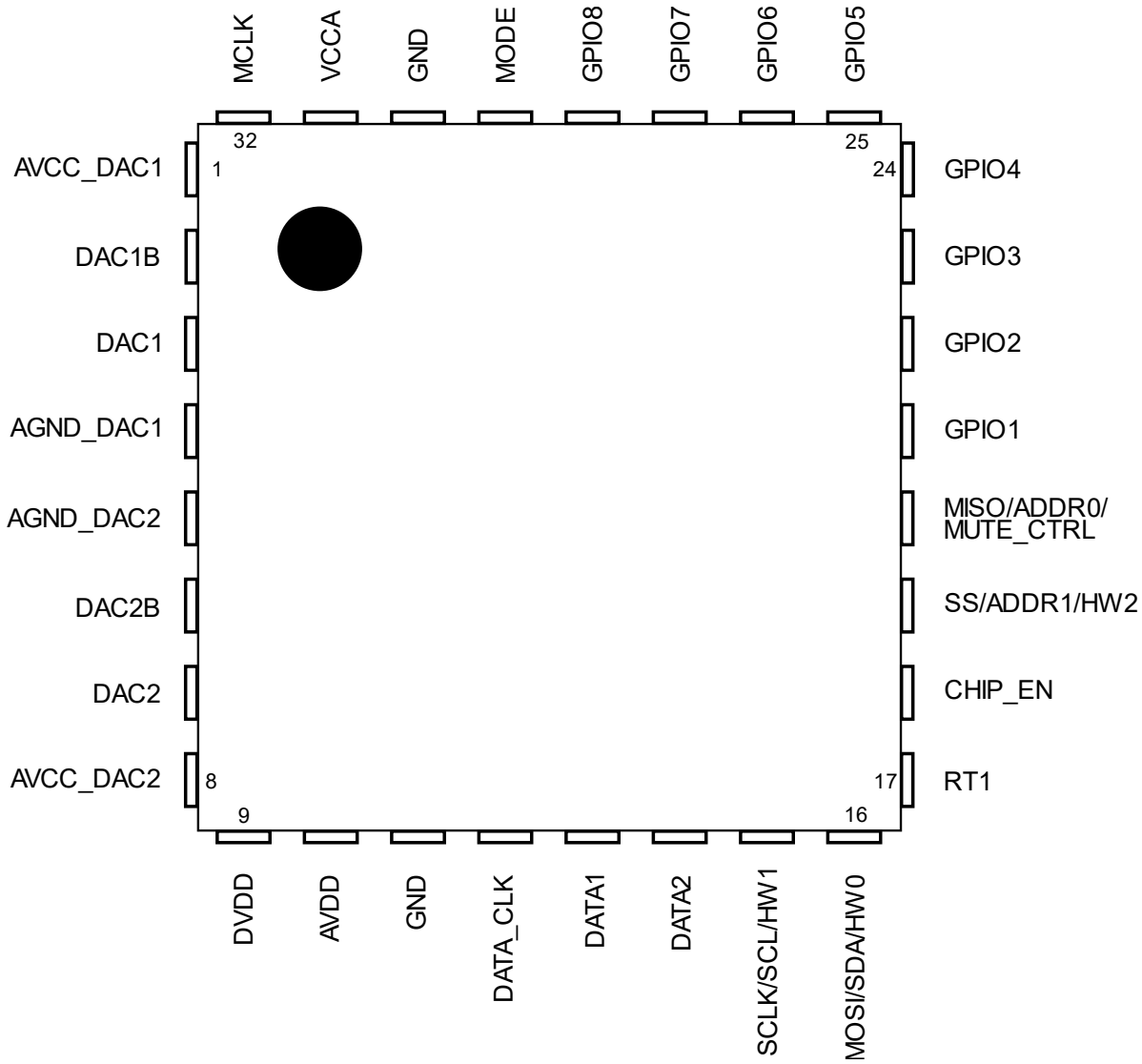


Figure 2 - ES9039Q2M Pinout

32 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	AVCC_DAC1	Power	Power	3.3V DAC analog output stage reference supply for the Channel 1
2	DAC1B	AO	Ground	Differential Negative Output for Channel 1
3	DAC1	AO	Ground	Differential Positive Output for Channel 1
4	AGND_DAC1	Ground	Ground	DAC analog output stage ground for Channel 1
5	AGND_DAC2	Ground	Ground	DAC analog output stage ground for Channel 2
6	DAC2B	AO	Ground	Differential Negative Output for Channel 2
7	DAC2	AO	Ground	Differential Positive Output for Channel 2
8	AVCC_DAC2	Power	Power	3.3V DAC analog output stage reference supply for the Channel 2
9	DVDD	Power	Power	Digital Supply, 1.2V (Internally Supplied)
10	AVDD	Power	Power	3.3V digital regulator supply
11	GND	Ground	Ground	Device Ground
12	DATA_CLK	I	HiZ	Serial Data Clock pin
13	DATA1	I	HiZ	Serial DATA1 pin
14	DATA2	I	HiZ	Serial DATA2 pin
15	SCLK	I	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
16	MOSI	I	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
17	RT1	I/O	HiZ	Reserved. Must be connected to GND for normal operation.
18	CHIP_EN	I/O	HiZ	Active-high Chip Enable
19	SS	I	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
20	MISO	I	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_CTRL			Hardware Mute Control pin, controlled by MODE
21	GPIO1	I/O	Ground	Automute Output, General I/O w/extended functions
22	GPIO2	I/O	Ground	Lock Status Output, General I/O w/extended functions
23	GPIO3	I/O	HiZ	General I/O w/extended functions
24	GPIO4	I/O	HiZ	General I/O w/extended functions
25	GPIO5	I/O	HiZ	General I/O w/extended functions
26	GPIO6	I/O	HiZ	General I/O w/extended functions
27	GPIO7	I/O	HiZ	General I/O w/extended functions
28	GPIO8	I/O	Res. to Ground**	Calibration Resistor & General I/O w/extended functions
29	MODE	I/O	HiZ	I²C/SPI Control selection or HW mode
30	GND	Ground	Ground	Device Ground
31	VCCA	Power	Power	Analog Supply, 3.3V
32	MCLK	I/O	HiZ	Oscillator input
33	External PAD[1]	-	-	External pad, connect to GND

Table 1 - 32 QFN Pin Descriptions

[1] Pin 33 is the package pad. See 32 QFN package dimensions for sizing. Connect to GND.

Feature List

The ES9039Q2M is a SABRE® 2 channel high performance digital to analog converter (DAC) with features and performance including the new Hyperstream IV modulator that produced a very high-performance device that is well suited for a variety of applications.

In addition to improved performance, the new ES9039Q2M SABRE DAC now supports the TDM audio interface, SPI (or I²C) control interface and hardware modes for simplifying device configuration.

TDM, I²S including LF & RJ, DSD & DoP audio interfaces are supported.

Sample rates up to 768kHz (@ 64FS Mode) with PCM data with 2 selectable digital filters to choose from and a programmable filter for custom sound signatures. DSD rates up to DSD1024 (512 x 44.1kHz) are also supported.

Configuration Modes

The ES9039Q2M has 4 control programming modes. They are controlled by the state of the MODE pin (Pin 29).

MODE PIN	Configuration
0	I²C Interface
Pull Low	HW control mode (see Hardware Mode Table)
Pull High	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Software Mode

The ES9039Q2M supports I²C or SPI serial communication to configure registers. There are two types of registers, read/write and read-only registers.

I²C

- MODE (Pin 29) - GND
- Connect per I²C standard
  - SDA (Pin 16)
  - SCL (Pin 15)
  - ADDR0 (Pin 20)
  - ADDR1 (Pin 19)

I²C Address	ADDR1	ADDR0
0x90	GND	GND
0x92	GND	AVDD
0x94	AVDD	GND
0x96	AVDD	AVDD

Table 3 - I²C Addresses

SPI

- MODE (Pin 29) - AVDD
- Connect per SPI standard
  - MOSI (Pin 16)
  - SCLK (Pin 15)
  - SS (Pin 19)
  - MISO (Pin 20)

SPI Command	First Byte
Write	3
Read	1

Table 4 - SPI Commands

Hardware Mode

The ES9039Q2M has pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

Note: All Synchronous hardware modes have Automatic FS (sample rate) detection enabled.

These modes are set with pins:

- MODE (Pin 29)
- HW0 (Pin 16)
- HW1 (Pin 15)
- HW2 (Pin 19)
- MUTE_CTRL (Pin 20)

Each hardware mode pin has 4 states:

- 0 - Pin directly connected to GND
- 1 - Pin directly connected to AVDD
- Pull 0 - Pin pulled to GND through 47kΩ resistor
- Pull 1 - Pin pulled to AVDD through 47kΩ resistor

In Hardware mode, most GPIOs have specific functions.

GPIO #	Input/Output	HW Mode Function
GPIO1	Output	Automute Status (AND of both channels)
GPIO2	Output	SRC Lock (Reg 249[2] register for readback)
GPIO3	Output	Daisy chain mode data output
GPIO4	Input	S/PDIF input in HW mode (HW modes 16-18)
GPIO5	Input	DoP HW enable: • 1'b0: DoP disabled • 1'b1: DoP enabled Note: Requires a PCM (I²S/LJ/TDM) HW mode to be selected
GPIO6	Input	FIR filter selection: • 1'b0: minimum phase (register default) • 1'b1: Linear phase fast roll-off Note: See section on Digital Filters for more information
GPIO7	Ground	Must be connected to Ground in HW mode (Pin 27)
GPIO8	Input	CAL_RES input (Calibration Resistor) See calibration section for more information

Table 5 - GPIO Function in Hardware Mode

Design Information

Each hardware mode pain can be configured with either a pull-up or pull-down resistor. Therefore, it is important that the pin is configured to allow for the desired hardware modes. Some guidelines include the following:

- The HW0 and HW1 pins never require a pull up or pull-down resistor.

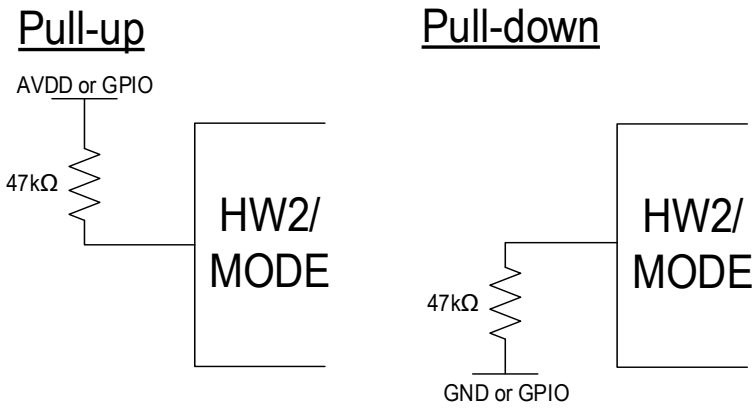


Figure 3 - Hardware Mode Pin Configurations

Muting

MUTE_CTRL (Pin 20) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

HW MUTE Control (Pin 20)	Condition
0	Output Muted, No Automute
1	Output Unmuted, No Automute
Pull 0	Output Muted, Automute Enabled
Pull 1	Output Unmuted, Automute Enabled

Table 6 - Mute Control for HW Mode Configuration

Hardware Mode Pin Configuration

The following table shows the available hardware modes for the ES9039Q2M. All Synchronous Hardware modes (HW) have Automatic FS detection enabled with FS & BCK being detected. See Register 3[7] for more details.

HW#	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes								
0	I²S Master	MCLK/128	MCLK/2 (64FS)	MCLK=128*FS ≤49.152	Pull 0	0	0	0
1	I²S Master	MCLK/256	MCLK/4 (64FS)	MCLK=256*FS ≤49.152	Pull 0	0	0	1
2	I²S Master	MCLK/512	MCLK/8 (64FS)	MCLK=512*FS ≤49.152	Pull 0	0	1	0
3	I²S Master	MCLK/1024	MCLK/16 (64FS)	MCLK=1024*FS ≤49.152	Pull 0	0	1	1
4	LJ Master Mode	MCLK/128	MCLK/2 (64FS)	MCLK=128*FS ≤49.152	Pull 0	Pull 0	0	0
5	LJ Master Mode	MCLK/256	MCLK/4 (64FS)	MCLK=256*FS ≤49.152	Pull 0	Pull 0	0	1
6	LJ Master Mode	MCLK/512	MCLK/8 (64FS)	MCLK=512*FS ≤49.152	Pull 0	Pull 0	1	0
7	LJ Master Mode	MCLK/1024	MCLK/16 (64FS)	MCLK=1024*FS ≤49.152	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes, SYNC								
8	I²S Slave, SYNC, MCLK/1	8<FS<768	64FS	64*FS≤MCLK ≤49.152	Pull 0	Pull 1	0	0
9	I²S Slave, SYNC, MCLK/2	8<FS<384	64FS	128*FS≤MCLK ≤49.152	Pull 0	Pull 1	0	1
10	I²S Slave, SYNC, MCLK/4	8<FS<192	64FS	256*FS≤MCLK ≤49.152	Pull 0	Pull 1	1	0
11	I²S Slave, SYNC, Auto Clock Gear[1] (128FS)	8<FS<384	64FS	64*FS≤MCLK ≤49.152	Pull 0	Pull 1	1	1
12	LJ Slave, SYNC, MCLK/1	8<FS<384	64FS	64*FS≤MCLK ≤49.152	Pull 0	1	0	0
13	LJ Slave, SYNC, MCLK/2	8<FS<384	64FS	128*FS≤MCLK ≤49.152	Pull 0	1	0	1
14	LJ Slave, SYNC, MCLK/4	8<FS<192	64FS	256*FS≤MCLK ≤49.152	Pull 0	1	1	0
15	LJ Slave, SYNC, Auto Clock Gear[1] (128FS)	8<FS<384	64FS	64*FS≤MCLK ≤49.152	Pull 0	1	1	1

Table 7 – Hardware Mode Pin Configurations Pt1

[1] ACG (Auto Clock Gearing) will gear MCLK down to 128*FS, unless 64*FS is required, or 2*DSDCLK in DSD modes.

HW#	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Slave Modes & S/PDIF, ASYNC								
16	S/PDIF[1], I²S Slave, DoP[2] ASYNC, MCLK/1	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	0	0	0
17	S/PDIF[1], I²S Slave, DoP[2] ASYNC, MCLK/2	8<FS<384	64FS	130*FS<MCLK ≤49.152	Pull 1	0	0	1
18	S/PDIF[1], I²S Slave, DoP[2] ASYNC,MCLK/4	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	0	1	0
19	I²S Slave, ASYNC, Auto Clock Gear[3] (>130FS)	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	0	1	1
20	LJ Slave, ASYNC, MCLK/1	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	Pull 0	0	0
21	LJ Slave, ASYNC, MCLK/2	8<FS<384	64FS	130*FS<MCLK ≤49.152	Pull 1	Pull 0	0	1
22	LJ Slave, ASYNC, MCLK/4	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	Pull 0	1	0
23	LJ Slave, ASYNC, Auto Clock Gear[3] (>130FS)	8<FS<384	64FS	130*FS≤MCLK ≤49.152	Pull 1	Pull 0	1	1
DSD & TDM LJ Slave Modes								
24	DSD Slave SYNC, MCLK/1	DSD64-512	2FS	4*FS ≤ MCLK ≤ 45.1584	Pull 1	Pull 1	0	0
25	DSD Slave SYNC, Auto Clock Gear (4*FS)	DSD64-512	2FS	4*FS ≤ MCLK ≤ 45.1584	Pull 1	Pull 1	0	1
26	DSD Slave ASYNC, MCLK/1	DSD64-512	2FS	6*FS ≤ MCLK ≤ 50	Pull 1	Pull 1	1	0
27	DSD Slave ASYNC, Auto Clock Gear (>6*FS)	DSD64-512	2FS	6*FS ≤ MCLK ≤ 50	Pull 1	Pull 1	1	1
28	TDM[4] LJ Slave SYNC, Autodetect (Slots 1 to 8)	8<FS<768	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	64*FS≤MCLK ≤49.152	Pull 1	1	0	0
29	TDM[4] LJ Slave SYNC, Autodetect (Slots 9 to 16)	8<FS<384	Auto (128FS, 256FS, 512FS, 1024FS)	128*FS≤MCLK ≤49.152	Pull 1	1	0	1
30	TDM[4] LJ Slave SYNC, Autodetect (Slots 17 to 24)	8<FS<192	Auto (256FS, 512FS, 1024FS)	256*FS≤MCLK ≤49.152	Pull 1	1	1	0
31	TDM[4] LJ Slave SYNC, Autodetect (Slots 25 to 32)	8<FS<192	Auto (256FS, 512FS, 1024FS)	256*FS≤MCLK ≤49.152	Pull 1	1	1	1

Table 8 – Hardware Mode Pin Configurations Pt2

Note: Mode 28 = Channel Slots 1&2, Mode 29 = Channel Slots 3&4, Mode 30 = Channel Slots 5&6, Mode 31 = Channel Slots 7&8

[1] For S/PDIF in HW mode, DATA7/GPIO7 is the S/PDIF stream input. The ES9039Q2M must be reset (CHIP_EN) when changing to and from S/PDIF.

[2] To enable DoP in HW mode, GPIO5 Pin must be high

[3] ACG (Auto Clock Gearing) is enabled, it will normally gear the clock down to 128*FS, unless 64*FS is required, or 2*DSDCLK in DSD modes.

[4] TDM uses auto channel detect to determine the amount of channels. 8 Channels of data on a single data line is required in hardware mode to map to all 8 DACs. In software mode, 4 channels on 2 data lines is also supported.

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized and after CHIP_EN is asserted, then asserted last.

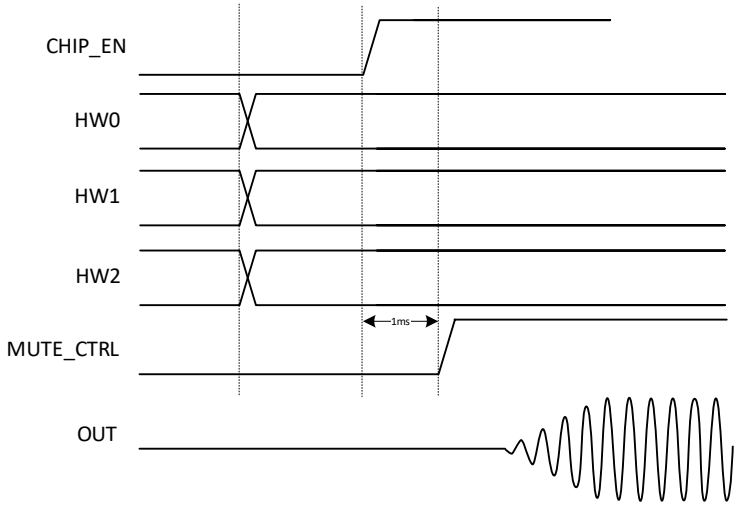


Figure 4 - Hardware Mode Startup Sequence

Digital Features

See Recommended Operating Conditions for additional information.

Digital Signal Path

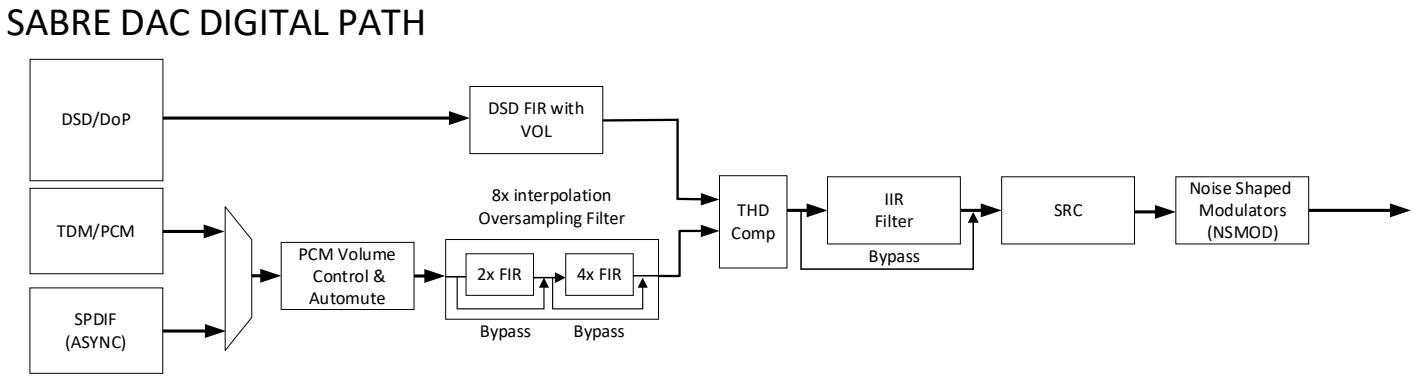


Figure 5 - Digital Signal Path

Volume Control

This volume control is intended for use during audio playback. Each channel can be digitally attenuated from 0dB to -127.5dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the DAC VOL UP RATE, DAC VOL DOWN RATE and DAV VOL DOWN RATE FAST registers.

Muting the DAC output can be accomplished by DAC_MUTE_CHx from Register 86.

Channel volumes, by default, are updated as soon as the volume registers are written. However, the volume control can be updated for both channels together by using VOLUME_HOLD.

Volume Control Registers

- Register 74: VOLUME CH1
- Register 75: VOLUME CH2
- Register 82: DAC VOL UP RATE
- Register 83: DAC VOL DOWN RATE
- Register 84: DAC VOL RATE DOWN FAST
- Register 89[4]: VOLUME_HOLD

Volume control is available for PCM (I²S, LJ, RJ, TDM), DoP (DSD over PCM), and DSD. There is separate control for each channel.

Automute

In HW mode automute is controlled by the state of the MUTE_CTRL pin (Pin 20), the pin must be “Pull 0” or “Pull 1” to enable automute.

In SW mode automute is enabled by default and can be disabled on each channel individually through Register 123 AUTOMUTE ENABLE.

The thresholds that engage and disengage automute can be configured through the AUTOMUTE LEVEL and AUTOMUTE OFF LEVEL registers.

If automute is enabled, it will be triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than automute_level for longer than the automute_time. Date is at a constant DC level for longer than automute_time.	$\frac{2\text{^}18}{(automute\_time * FS)}$
DoP/DSD	DSD data contains a DSD mute pattern (equal number of 1’s and 0’s in 8 consecutive bits of data), for longer than automute_time. DSD data contains all 1’s or 0’s in 8 consecutive bits of data, for longer than automute_time.	$\frac{2\text{^}18}{(automute\_time * FS)}$

Table 9 - Automute Configuration

Automute Configuration Registers

- Register 123: AUTOMUTE ENABLE
- Register 124-125: AUTOMUTE TIME
- Register 126-127: AUTOMUTE LEVEL
- Register 128-129: AUTOMUTE OFF LEVEL
- Register 62[7]: DISABLE_DSD_DC - Disables the DSD automute condition for 8 consecutive bits of 1’b1 or 1’b0
- Register 62[6]: DISABLE_DSD_MUTE - Disables the DSD automute condition for the DSD Mute pattern
- Register 62[0]: DISABLE_PCM_IC - Disables the PCM automute condition for a constant DC level

8x FIR Interpolation Oversampling Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filter shapes (Register 88[2:0] FILTER_SHAPE) or custom sound signatures can be programmed.

For more information on filters see Digital Filters section.

THD Compensation

The ES9039Q2M has built-in THD compensation to help compensate for system second and third harmonics that may be present on the output signal. The compensation is controlled through 4 individual signed 16-bit coefficients in the THD Compensation Coefficient Registers.

The following equation displays how the second and third harmonics are affected by the C2 and C3 values:

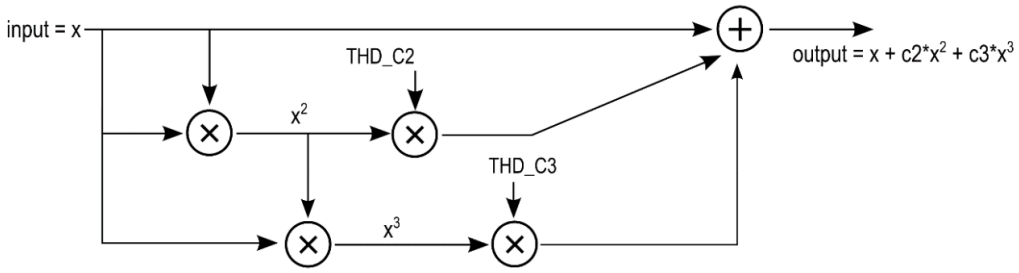


Figure 6 - THD Compensation Block Diagram

THD Compensation Coefficient Registers

- Registers 94-93: THD_C2_CH2 THD Compensation for C2 for Channel 2
- Registers 92-91: THD_C2_CH1 THD Compensation for C2 for Channel 1
- Registers 110-109: THD_C3_CH2 THD Compensation for C3 for Channel 2
- Registers 108-107: THD_C3_CH1 THD Compensation for C3 for Channel 1

Note: Coefficients are 16-bit signed values

IIR Filter

The IIR filter in the ES9039Q2M can be bypassed by using Register 90[2]: IIR_BYPASS.

The bandwidth of the filter is controlled by Register 89[2:0]: IIR_BW

GPIO Software Configuration

Each GPIO from 1 to 8 has 14 configurable modes (mode 8 & 15 are reserved). The table below shows the available configurations. See GPIO pin descriptions for Hardware and Software mode setups.

GPIO#_CFG	Function	Input / Output	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8
4'd0	Analog Shutdown	Output	Shutdown							
4'd1	Output 0	Output	Output 0							
4'd2	Output 1	Output	Output 1							
4'd3	Clocks	Output	CLKEN_1FS	CLK_BCK	CLK_DAC	CLK_IDAC	CLKEN_1FS	CLK_BCK	CLK_DAC	CLK_IDAC
4'd4	Interrupt	Output	OR of all interrupts							
4'd5	Mute	Input	Mute all channels							
4'd6	System Mode Control	Input	See System mode control section							
4'd7	SRC lock status	Output	src_locked flag							
4'd8	-	-	Reserved							
4'd9	PWM1 signal	Output	PWM1 signal							
4'd10	PWM2 signal	Output	PWM2 signal							
4'd11	PWM3 signal	Output	PWM3 signal							
4'd12	Minimum volume[1]	Output	vol_min flag							
4'd13	Automute status[2]	Output	dac_automute flag							
4'd14	Soft ramp done[2]	Output	dac_ss_ramp flag							
4'd15	-	-	Reserved							

Table 10 - GPIO Configuration Function

[1] Can be bitwise ANDed, ORed, or a specifical channel output; based on the values of Registers 46-47[6:0].

GPIO Configuration Descriptions

Analog Shutdown
Output shutdown

Output 0
Outputs a constant 1'b0

Output 1
Outputs a constant 1'b1

Clocks

- GPIO1: CLKEN_1FS (1*FS pulse clock)
- GPIO2: CLK_BCK
- GPIO3: CLK_DAC (SYS_CLK)
- GPIO4: CLK_IDAC (128*FS clock)
- GPIO5: CLKEN_1FS
- GPIO6: CLK_BCK
- GPIO7: CLK_DAC
- GPIO8: CLK_IDAC

Interrupt
Bitwise OR of all masked interrupts. See Register 10-21 for interrupt descriptions.

Mute
Mute all DAC channels.

System Mode Control
Works with Registers 46-47[15]: GPIO_DAC_MODE

When any GPIOx_CFG = 4'b6 (system mode control):

- 1'b0: Disable datapath when GPIOx input is 1'b1
- 1'b1: Enable datapath when GPIOx input is 1'b1

When GPIOx input is 1'b0, system mode is determined by Register 0[1]: DAC_MODE_REG

SRC Lock Status
SRC (Sample Rate Converter) lock status output. If the device is in a synchronous mode, output will be 1'b0.

PWM Signals

Outputs 1 of 3 PWM signals. Frequency and duty cycle on the PWM signals can be calculated with the following equations:

$$frequency[Hz] = \frac{SYS\_CLK}{PWM\#\_FREQ + 1}$$

$$Duty\ Cycle[\%] = \left(\frac{PWM\#\_COUNT}{PWM\#\_FREQ + 1}\right) x100$$

Each PWM signal can be controlled by the following Registers:

- PWM1: Register 48 PWM1_COUNT, Register 49-50 PWM1_FREQ
- PWM2: Register 51 PWM2_COUNT, Register 52-53 PWM2_FREQ
- PWM3: Register 54 PWM3_COUNT, Register 55-56 PWM3_FREQ

Minimum Volume

VOL_MIN flag output is high during normal and abnormal mute conditions.

Normal mute conditions: register mute, gpio mute, override mute, and automute.
Abnormal mute conditions: loss of SRC lock, and BCK_WS_FAIL

Register 46-47[1]: GPIO_AND_VOL_MIN sets the GPIO output to be the logical AND of all channel VOL_MIN flags. Overrides GPIO_OR_VOL_MIN.

Register 46-47[4]: GPIO_OR_VOL_MIN sets the GPIO output to be the logical OR of all channel VOL_MIN flags.

Register 46-47[6]: GPIO_SEL will output the flag of a specific channel if GPIO_OR_VOL_MIN and GPIO_AND_VOL_MIN are both 1'b0.

Automute Status

DAC_AUTOMUTE flag output is high when automute is active.

Register 46-47[0]: GPIO_AND_AUTOMUTE sets the GPIO output to be the logical AND of all channel DAC_AUTOMUTE flags.

Register 46-47[3]: GPIO_OR_AUTOMUTE set the GPIO output to be the logical OR of all channel DAC_AUTOMUTE flags.

Register 46-47[6]: GPIO_SEL will output the flag of a specific channel if GPIO_OR_AUTOMUTE and GPIO_AND_AUTOMUTE are both 1'b0.

Soft Ramp Done

DAC_SS_RAMP flag output is high when the ES9039Q2M is not in the process of ramping either up or down.

Register 46-47[2]: GPIO_AND_SS_RAMP sets the GPIO output to be the logical AND of all channel DAC_SS_RAMP flags.

Register 46-47[5]: GPIO_OR_SS_RAMP sets the GPIO output to be the logical OR of all channel DAC_SS_RAMP flags.

Register 46-47[6]: GPIO_SEL will output the flag of a specific channel if GPIO_OR_SS_RAMP and GPIO_AND_SS_RAMP are both 1'b0.

GPIO Pin Descriptions

GPIOx	Hardware Mode	Software mode
GPIO1	Automute status.	Regular GPIO
GPIO2	Lock Status	Regular GPIO
GPIO3	No hardware mode connection	GPIO3 is connected to the Reg60[5] *TDM_DAISY_CHAIN* logic. When *TDM_DAISY_CHAIN* = 1'b1, GPIO3 can ONLY be used as an output for daisy chain delayed data line. If TDM_DAISY_CHAIN = 1'b0, GPIO3 can then be used as a GPIO.
GPIO4	S/PDIF input pin, requires HW modes 16-18.	Regular GPIO.
GPIO5	DoP input enable, requires HW modes 0-23, 28-31	Regular GPIO.
GPIO6	FIR filter selection, 1'b0: Filter 0, Minimum phase (register default), 1'b1: Filter 2, Linear phase fast roll-off. Requires HW modes 0-23, 28-31.	Regular GPIO.
GPIO7	Connect to Ground*	Regular GPIO.
GPIO8	CAL_RES (calibration resistor)	CAL_RES, disable to use as regular GPIO.

Note*: In Hardware mode GPIO7 needs to be connected to Ground.

Audio Input Formats

The ES9039Q2M supports multiple serial input data formats. Input format is selected either through Hardware Mode or Software Mode (Register 1:SYS MODE CONFIG).

The ES9039Q2M can automatically determine the input data format by enabling Register 57[0]: AUTO_INPUT_SEL, data must be provided on the DATA2 pin, to properly decode the input format. The input data format can also be selected using Register 57[2:1]: INPUT_SEL.

For Hardware Mode see hardware mode for inputs.

The formats include:

- PCM
  - Slave and master mode in 16, 24, and 32-bit widths
  - I²S, Left Justified (LJ), and Right Justified (RJ)
  - TDM up to TDM1024 mode with 32 slots including daisy chain mode
  - Sample rates up to 768kHz (64fs mode)
  - Channel Remapping & Invert
- DoP (DSD Over PCM)
  - Slave and master mode
  - Sample rates up to DoP512 (24bit, 1.4112MHz PCM)
  - Channel Remapping & Invert
- Native DSD
  - Slave and master mode
  - Sample rates from DSD64 (2.8224Mbits/sec, 64 x 44.1kHz) to DSD1024
  - Channel Remapping & Invert
- S/PDIF
  - Selectable input pin and payload information
  - S/PDIF input in HW mode (HW modes 16-18) using GPIO4

PCM (I²S, LJ, RJ)

Data is organized into 2 channels per data line. Any channel on any data line can be mapped to any DAC through the TDM_CHx_CONFIG channel mapping Registers 64-65. Data is latched on the positive edge of BCLK.

PCM Pin Connections (default configuration):

Pin Name	Function	Description
DATA_CLK	I²S BCLK	I²S Clock (Bit Clock), Master or Slave
DATA1	I²S WS	I²S WS (Word Select/Frame Select), Master or Slave
DATA2	I²S DATA	I²S Data

Table 11 - PCM Pin Connections

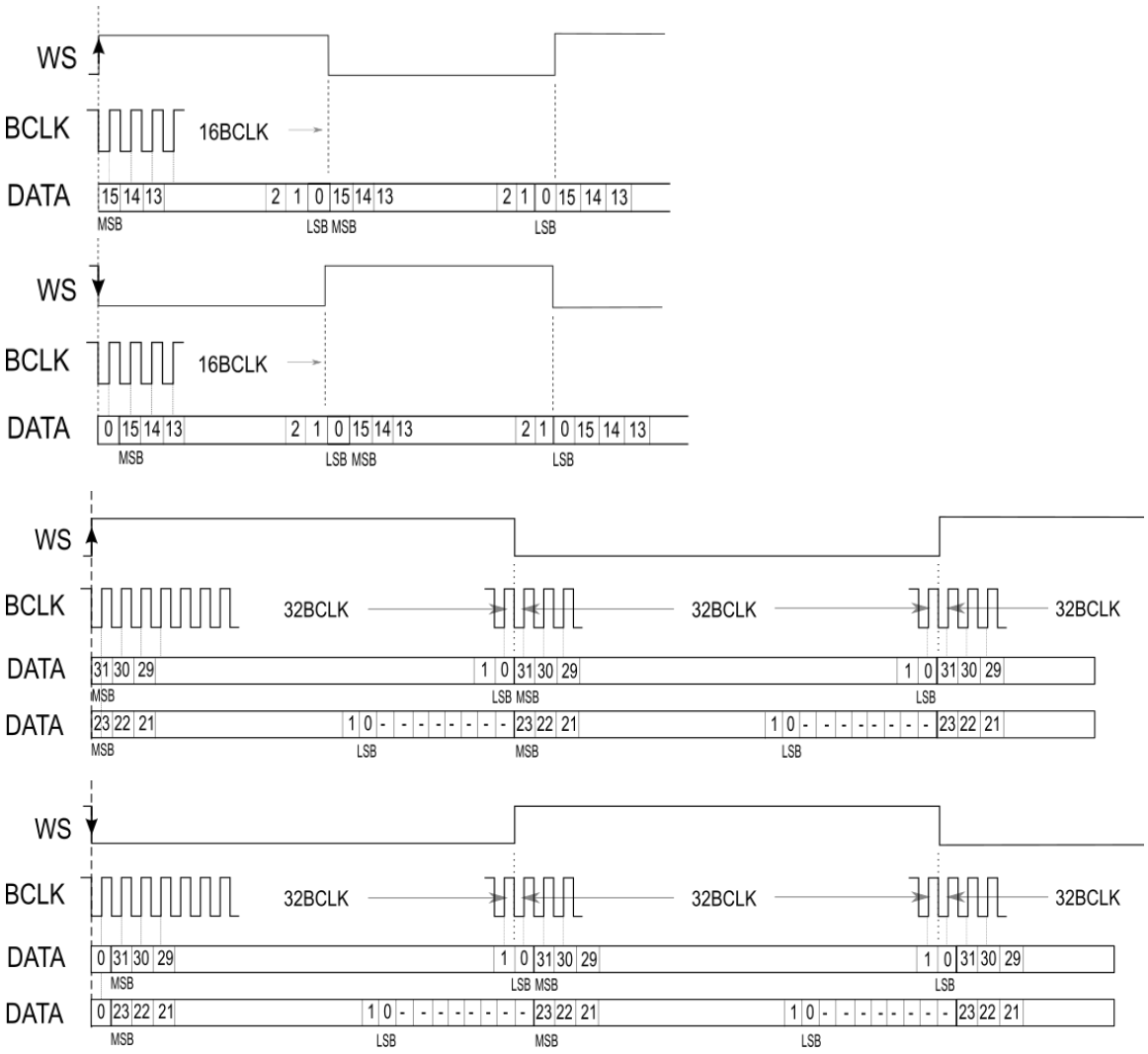


Figure 7 - LJ & I²S Input for 16bit and 32bit Word Depths

Note: RJ is supported but only in software mode.

TDM (Time-Division Multiplexing)

The ES9039Q2M supports time-division multiplexing (TDM) format, allowing more than 2 channels (or slots) to be transmitted on each data line, up to a maximum of 32 channels per data line. Typical formats are TDM128 (4chx32bit), TDM256 (8chx32bit), TDM512 (16chx32bit) and TDM1024 (32chx32bit). In this mode, Registers 64[4:0] & 65[4:0] PCM_CHx_SLOT_SEL can be used to internally map any TDM slot (channel) to either DAC. Data is latched on the positive edge of BCLK.

TDM Pin Connection (default configuration)

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM Clock, Master or Slave
DATA1	TDM WS	TDM WS (Word Select/Frame Select), Master or Slave
DATA2	TDM DATA	TDM DATA

Table 12 - TDM Pin Connections

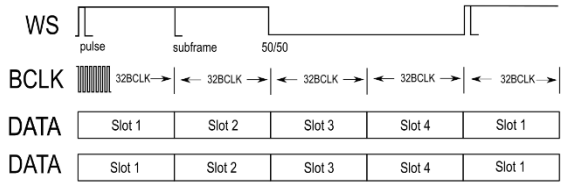


Figure 8 - TDM128 Mode

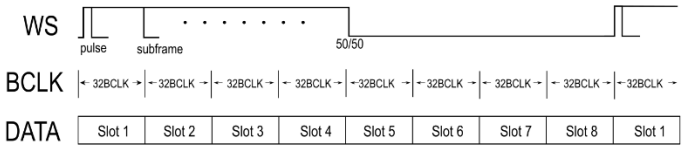


Figure 9 - TDM256 Mode

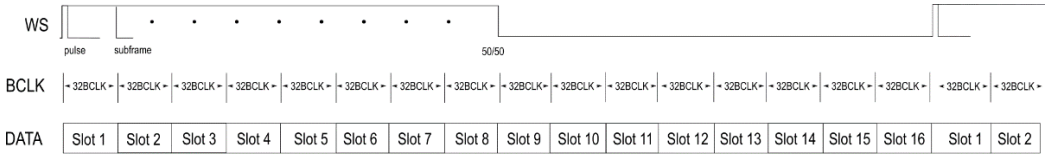


Figure 10 - TDM512 Mode

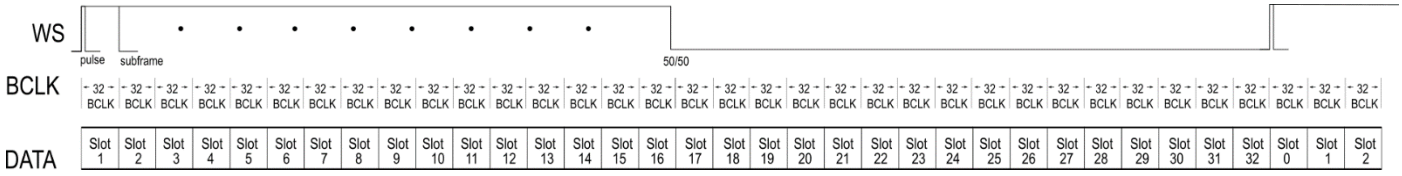


Figure 11 - TDM1024 Mode

Multiple ES9039Q2M Devices in Parallel in TDM Mode

In TDM modes, several ES9039Q2M can be used in parallel to increase the number of channels. Each ES9039Q2M can be configured in HW or SW mode to output its data to different slots on the TDM DATA line.
Note: in Hardware modes, only Left Justified TDM formats are supported. In Software mode, the user can configure it to be I²S TDM format.

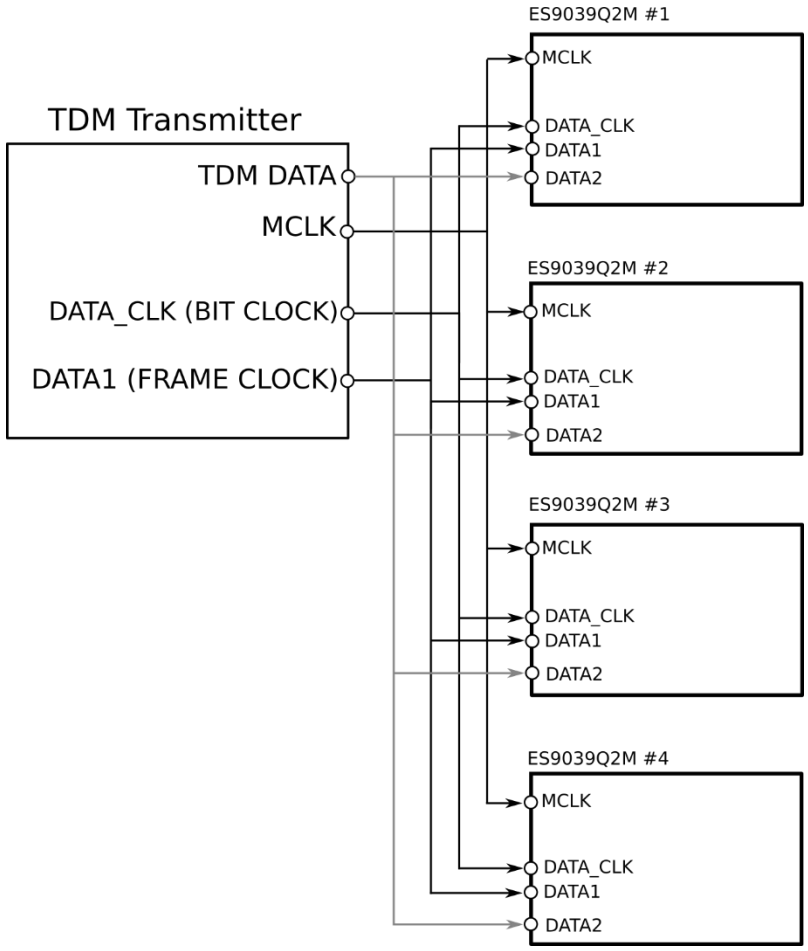


Figure 12 - TDM Connection of Several ES9039Q2M Devices in Parallel

Applicable Registers

- Register 60[7]: TDM_LJ_MODE set to 1'b1
- Register 60[6]: TDM_VALID_EDGE set to 1'b1
- Register 59[4:0]: TMD_CH_NUM
    - Or using Register 57[7]: AUTO_CH_DETECT
- Register 64-65[4:0]: PCM_CHx_SLOT_SEL, sets the TDM slots for each device

Daisy Chain Multiple ES9039Q2M Devices in TDM Mode

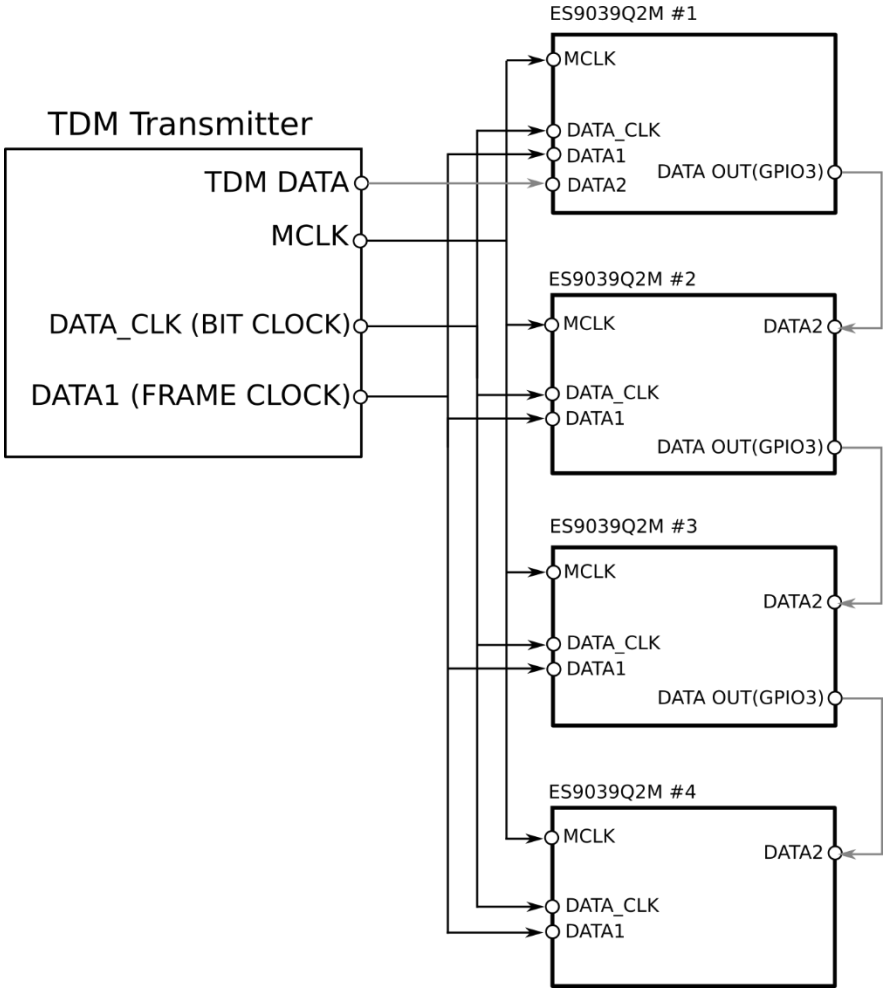


Figure 13 - TDM Connection of Several ES9039Q2M Devices in Daisy Chain Mode

Applicable Registers (Daisy chain mode is only available in software mode)

- Register 60[7]: TDM_LJ_MODE set to 1'b1
- Register 60[6]: TDM_VALID_EDGE set to 1'b1
- Register 60[5]: TDM_DAISY_CHAIN: Enables Daisy Chain mode
  - GPIO3 will output data pass-through on DATA2 line delayed by 1 BCLK
- Register 59[4:0]: TDM_CH_NUM or using Register 57[7]: AUTO_CH_DETECT: Sets the # of TDM slots / frame
- Register 61[4:0]: TDM_DATA_LATCH_ADJ: Sets the position of the start bit within each TDM slot
  - Value corresponds to the position of the device in the chain (zero-indexed)
- Register 64-65[4:0]: PCM_CHx_SLOT_SEL: Sets the TDM slots for each device
  - Note: The first chip in the chain is required to be in the final 2 slots

Note: An application note for Daisy Chain mode and TDM in general will be available shortly from ESS FAEs or your local distributor

DSD

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. There is no internal channel mapping for DSD input, DSD data input to DATA1 is sent to Ch1, DSD data input to DATA2 is sent to Ch2.

DSD Pin Connections (default configuration)

Pin Name	Function	Description
DATA_CLK	DSD Clock	DSD Clock Input
DATA1	DSD CH1	DSD DATA Channel 1
DATA2	DSD CH2	DSD DATA Channel 2

Table 13 - DSD Pin Connections

Automute is available for DSD once a constant DC level (8 1's or 8 0's in a row) is detected. The ES9039Q2M will then automute to the proper DSD mute pattern.

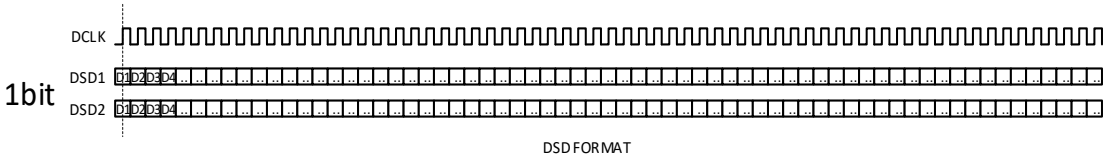


Figure 14 - DSD Format, 1-bit Stream

The ES9039Q2M can accept DS data line for multiple pins. The pins can be chosen using:

- Register 64[7:5]: DSD_CH1_SOURCE, DATA1 (default)
- Register 65[7:5]: DSD_CH2_SOURCE, DATA2 (default)

S/PDIF

S/PDIF Input

Pin Name	Description
GPIO4	HW mode 16-18 S/PDIF stream input
GPIOx or DATA1/2	Input selection from SPDIF_SEL for software mode

Table 14 - S/PDIF Pin Connections

S/PDIF is transmitted over a single signal line sing dual phase encoded data, which allows for clock extraction from the data signal line.

The ES9039Q2M has an integrated S/PDIF decoder that can be accessed in either Asynchronous Hardware or Software modes.

- For Hardware mode, the S/PDIF input is on GPIO4 using HW mode 16-18
  - S/PDIF unput stream must be disconnected in order to use other input formats
- For Software mode, the applicable registers are:
  - Register 89[7:4]: SPDIF_SEL
    - Selects the S/PDIF input pin
    - If a GPIO is selected, GPIO pins also require the GPIOx_SDB input to be enabled
  - Register 136[4:0]: SPDIF_DATA_SEL
    - Selects the byte of the S/PDIF payload in Register 251[7:0]: SPDIF_DATA_READ
  - Register 251 SPDIF_DATA_READ
    - Readback the payload, 24 bytes total

For decoding the S/PDIF payload see Channel Status Table below:

SPDIF CHANNEL STATUS - Consumer Configuration								
Address Offset (Bytes)	**[7]**	**[6]**	**[5]**	**[4]**	**[3]**	**[2]**	**[1]**	**[0]**
0	Reserved	Reserved	0: 2 Channel 1: 4 Channel	Reserved	0: No-Preemph 1: Preemph	0: CopyRight 1: Non-CopyRight	0: Audio 1: Data	0: Consumer 1: Professional
1	Category Code 0x00: General 0x01: Laser-Optical 0x02: DVD Converter 0x03: Magnetic 0x04: Digital Broadcast 0x05: Musical Instrument 0x06: Present A/D Converter 0x08: Solid State Memory 0x16: Future A/D Converter 0x19: DVD 0x40: Experimental							
2	Channel Number 0x0: Don't Care 0x1: A (Left) 0x2: B (Right) 0x3: C 0x4: D 0x5: E 0x6: F 0x7: G 0x8: H 0x9: I 0xA: J 0xB: K 0xC: L 0xD: M 0xE: N 0xD: O				Source Number 0x0: Don't Care 0x1: 1 0x2: 2 0x3: 3 0x4: 4 0x5: 5 0x6: 6 0x7: 7 0x8: 8 0x9: 9 0xA: 10 0xB: 11 0xC: 12 0xD: 13 0xE: 14 0xD: 15			
3	Reserved	Reserved	Clock Accuracy 0x0: Level 2 ±1000ppm 0x1: Level 1 ±50ppm 0x2: Level 3 variable pitch shifted		Sample Frequency 0x0: 44.1k 0x2: 48k 0x3: 32k 0x4: 22.05k 0x6: 24k 0x8: 88.2k 0xA: 96k 0xC: 176.4k 0xE: 192k			
4	Reserved	Reserved	Reserved	Reserved	Word Length: If Word Field Size = 0 000 = Not Indicated 100 = 19 bits 010 = 18 bits 110 = 17 bits 001 = 16 bits 101 = 20 bits	If Word Field Size = 1 000 = Not Indicated 100 = 23 bits 010 = 22 bits 110 = 21 bits 001 = 20 bits 101 = 24 bits		Word Field Size 0: Max 20 bits 1: Max 24 bits
5-23	Reserved							

Table 15 - S/PDIF Channel Status - Consumer Configuration

SPDIF CHANNEL STATUS - Professional Configuration								
Address Offset (Bytes)	**[7]**	**[6]**	**[5]**	**[4]**	**[3]**	**[2]**	**[1]**	**[0]**
0	Sampling Frequency: 00: Not Indicated (or see byte 4) 10: 48kHz 01: 44.1kHz 11: 32kHz		Lock: 0: Locked 1: Unlocked	Emphasis: 000: Emphasis not Indicated 001: No Emphasis 011: CD-Type Emphasis 111: J-17 Emphasis			0: Audio 1: Non-Audio	0: Consumer 1: Professional
1	User Bit Management: 0000: No Indication 1000: 192-bit Block as Channel Status 0100: As Defined in AES18 1100: User-Defined 0010: As in IEC60958-3 (consumer)				Channel Mode: 0000: Not Indicated (default to 2 ch) 1000: 2 Channel 0100: 1 Channel (monophonic) 1100: Primary / Secondary 0010: Stereo 1010: Reserved for User Applications 0110: Reserved for User Applications 1110: SCDSR (see byte 3 for ID) 0001: SCDSR (stereo left) 1001: SCDSR (stereo right) 1111: Multichannel (see byte 3 for ID)			
2	Alignment Level: 00: Not Indicated 10: -20dBFS 01: -18.06dBFS		Source Word Length: If Max = 20 bits 000 = Not Indicated 100 = 19 bits 010 = 18 bits 110 = 17 bits 001 = 16 bits 101 = 20 bits	If Max = 24 bits 000 = Not Indicated 100 = 23 bits 010 = 22 bits 110 = 21 bits 001 = 20 bits 101 = 24 bits		Use of Aux Sample Word: 000: Not Defined, Audio Max 20 bits 100: Used for Main Audio, Max 24 bits 010: Used for Coord, Audio Max 20 bits 110: Reserved		
3	Channel Identification: If bit 7 = 0 then channel number is 1 plus the numeric value of bits 0-6 (bit reserved). If bit 7 = 1 then bits 4-6 define a multichannel mode and bits 0-3 (bit reserved) give the channel number within that mode.							
4	FS Scaling: 0: No Scaling 1: Apply Factor of 1/1.001 to Value	Sample Frequency (FS): 0000: Not Indicated 0001: 24kHz 0010: 96kHz 1001: 22.05kHz 1010: 88.2kHz 1011: 176.4kHz 0011: 192kHz 1111: User defined				Reserved	DARS (Digital Audio Reference Signal) 00: Not a DARS 01: DARS Grade 2 (±10ppm) 10: DARS Grade 1 (±1ppm) 11: Reserved	
5	Reserved							
6-9	Alphanumerical Channel Origin: Four-Character Label using 7-bit ASCII with no Parity. Bits 55, 63, 71, 79 = 0.							
10-13	Alphanumerical Channel Destination: Four-Character Label using 7-bit ASCII with no Parity. Bits 87, 95, 103, 111 = 0.							
14-17	Local Simple Address Code: 32-bit Binary Number Representing the Sample Count of the First Sample of the Channel Status Block							
18-21	Time of Dat Code: 32-bit Binary Number Representing the Time of Source Encoding in Sample Since Midnight							
22	Reliability Flags 0: Data in Byte Range is Reliable 1: Data in Byte Range is Unreliable							
23	CRCC 00000000: Not Implemented X: Error Check Code for bits 0-183							

Table 16 - S/PDIF Channel Status - Professional Configuration

Digital Filters

The ES9039Q2M has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 88[2:0] FILTER_SHAPE for configuration)

#	Filter	Description
0	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#5) with less ripple and more image rejection
1	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
2	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
3	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
4	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
5	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
6	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
7	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 17 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

Customizable Programmable FIR Filters

The ES9039Q2M has an 8x interpolation oversampling FIT filter that is programmable. It is a combination of 2 filters, a 4x FIR filter and a 2x FIR filter.

These filters can be bypassed using Register 90[1] BYPASS_FIR4X & 90[0] BYPASS_FIR2X, which will source data to the IIR filter. It is recommended to use an 8xFS input if the bypass is used. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I²S, LJ or RJ format.

The addresses for the two filters are:

- 2x FIR, Address 0x00 - 0x7F (0 - 127), 128 coefficients
- 4x FIR, Address 0x80 - 0x9F (128 - 159), 32 coefficients

To program the filters, the following registers are required:

- Register 135: PROGRAM RAM CONTROL
  - [1] PROG_COEFF_WE
    - Enables writing to the programable coefficient RAM
  - [0] PROG_COEFF_EN
    - Use the built-in filters or custom filter
- Register 137: PROGRAM RAM ADDRESS
  - [7] PROG_COEFF_STAGE
    - Choose which FIT stage to write to, either 4x or 2x
  - [6:0] PROG_COEFF_ADDR
    - Selects the coefficient address when writing custom coefficients for the interpolation oversampling filter
- Register 140-138: PROGRAM RAW DATA
  - 24-bit signed filter coefficient to the address defined by PROG_COEFF_ADDR
- Register 248-246: PROG COEFF OUT READ
  - Used to readback the programmed coefficients

An example sequence of programming a coefficient into RAM:

```
Write Reg 137 0        // RAM Address = 0, 2x stage
Write Reg 138 32       // Set data bits [7:0] of 24 bit coefficient
Write Reg 139 255      // Set data bits [15:8]
Write Reg 140 255      // Set data bits [23:16]
Write Reg 135 0x02     // Write 24 bit coefficient to RAM
Write Reg 135 0x00     // Reset write enable
```

Repeat for all 4x and 2x coefficient addresses.

An application note the programming sequence and sample code will be available shortly from your ESS Distributor or FAE.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for the external processing time to serialize the data stream.

Digital Filter	Delay(us) @ FS = 44.1kHz
Minimum Phase (default)	174us
Linear Phase Apodizing Fast Roll-Off	840us
Linear Phase Fast Roll-Off	854us
Linear Phase Fast Roll-Off Low-Ripple	808us
Linear Phase Slow Roll-Off	229us
Minimum Phase Fast Roll-Off	174us
Minimum Phase Slow Roll-Off	152us
Minimum Phase Fast Roll-Off Low Dispersion	310us

Table 18 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45FS	Hz
Stop band	-96dB	0.55FS			Hz
Group Delay		2.91/FS		9.01/FS	s
Flatness (ripple)	0.0012				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41FS	Hz
Stop band	-107dB	0.50FS			Hz
Group Delay			32.81/FS		s
Flatness (ripple)	0.0027				dB

Linear Phase Fast Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45FS	Hz
Stop band	-115dB	0.55FS			Hz
Group Delay			33.43/FS		s
Flatness (ripple)	0.0031				dB

Linear Phase Fast Roll-off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-97dB	0.55FS			Hz
Group Delay			31.37/FS		s
Flatness (ripple)	0.0012				dB

Linear Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.44FS	Hz
Stop band	-90dB	0.75FS			Hz
Group Delay			5.87/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-99dB	0.55FS			Hz
Group Delay		2.91/FS		9.14/FS	s
Flatness (ripple)	0.0023				dB

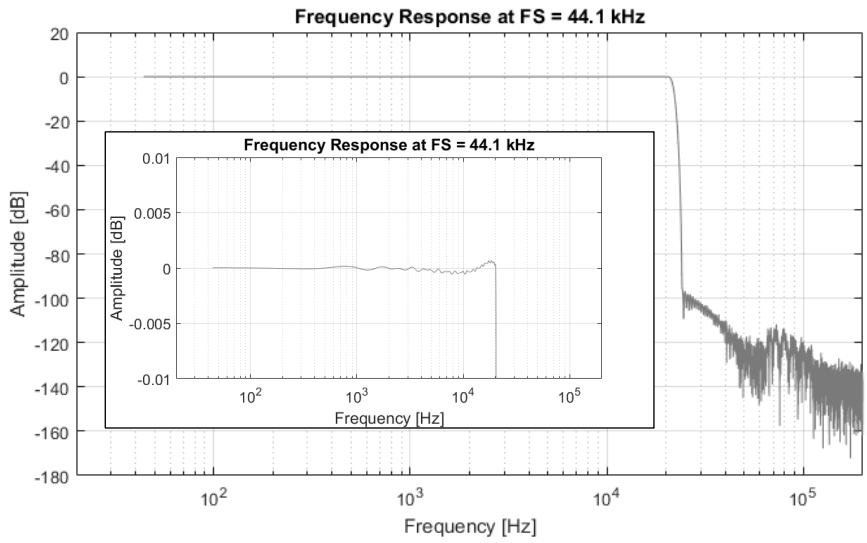
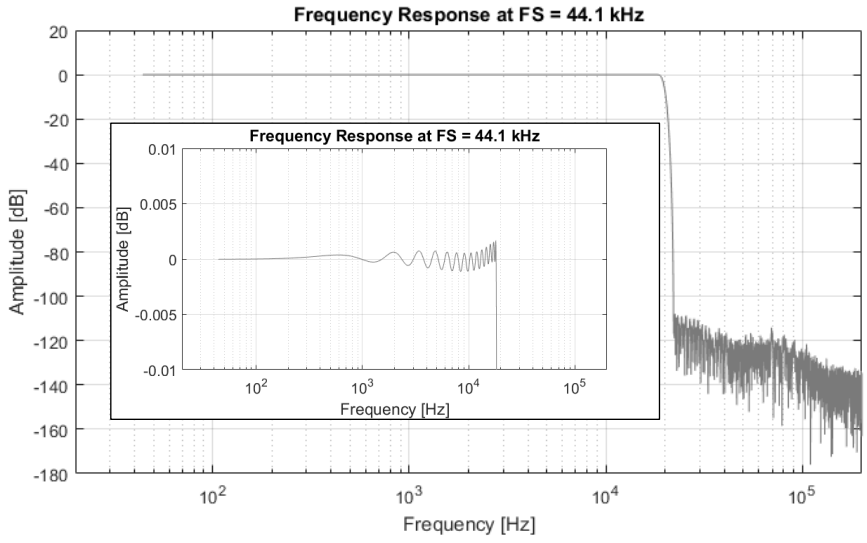
Minimum Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43FS	Hz
Stop band	-91dB	0.80FS			Hz
Group Delay		2.08/FS		3.56/FS	s
Flatness (ripple)					dB

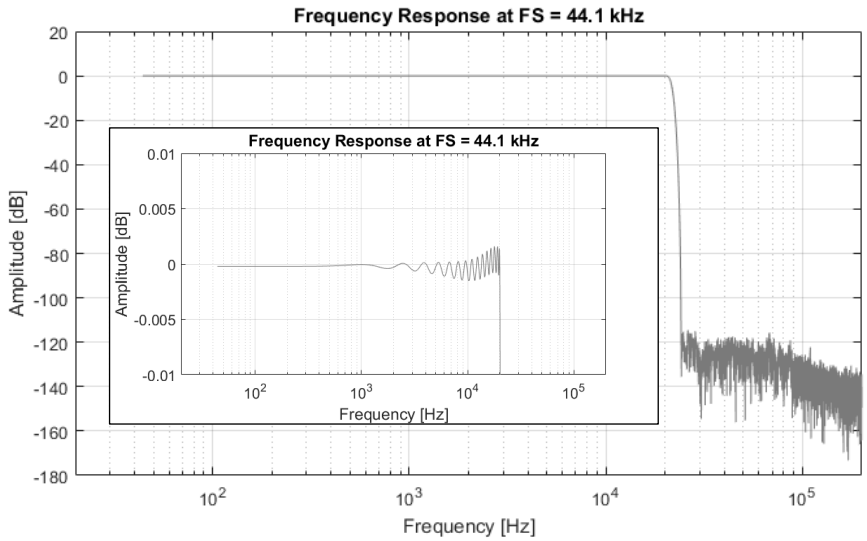
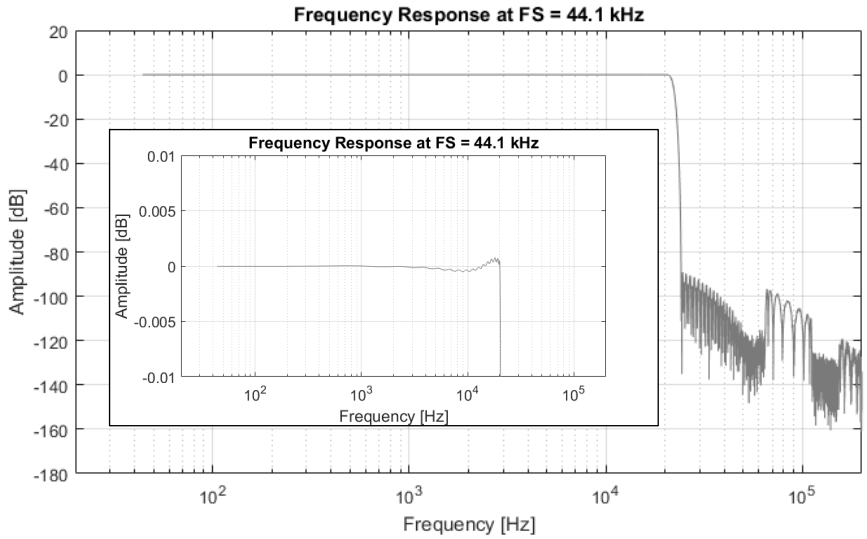
Minimum Phase Slow Roll-off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43FS	Hz
Stop band	-90dB	0.80FS			Hz
Group Delay		9.23/FS		9.75/FS	s
Flatness (ripple)					dB

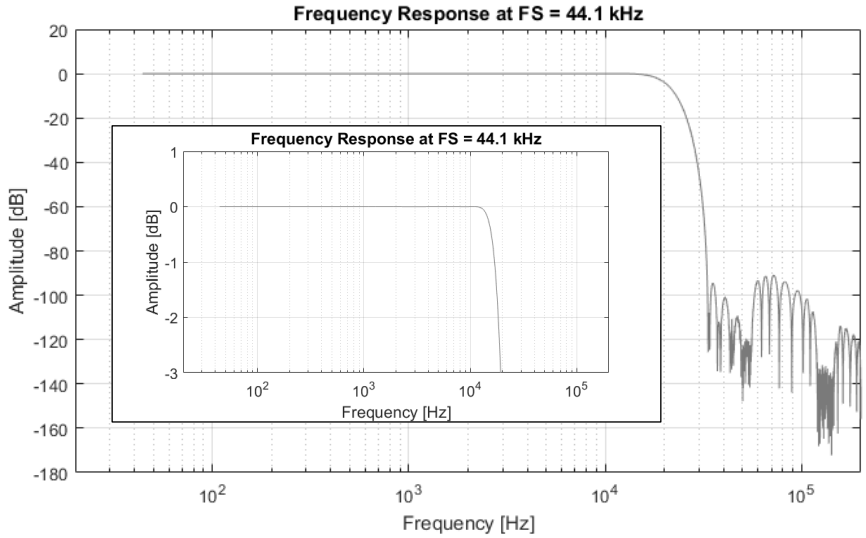
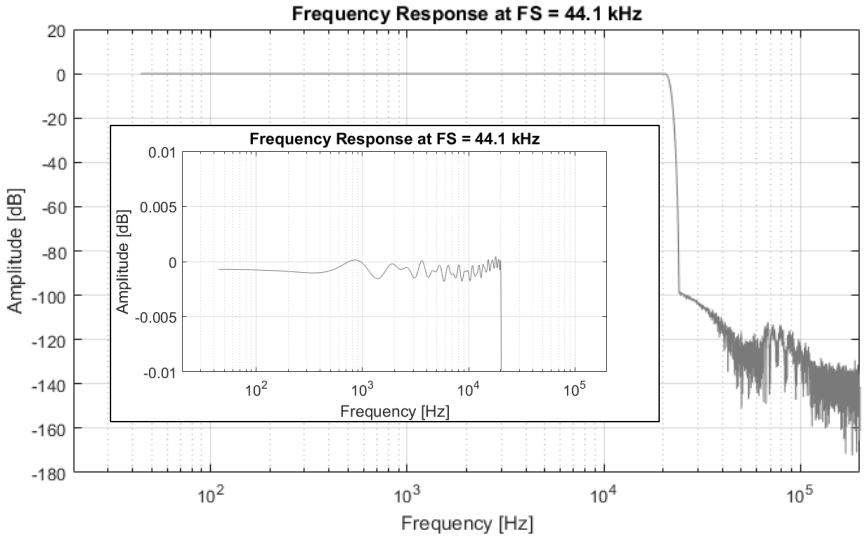
Table 19 - PCM Filter Properties

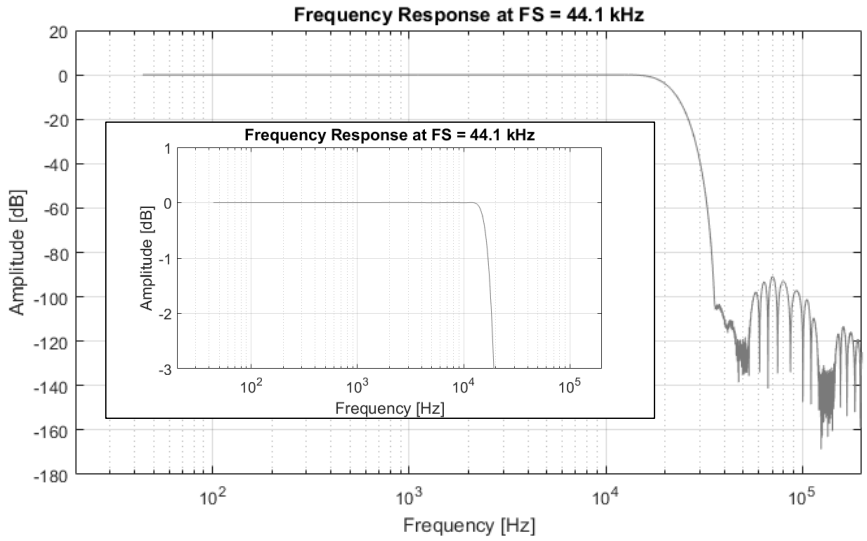
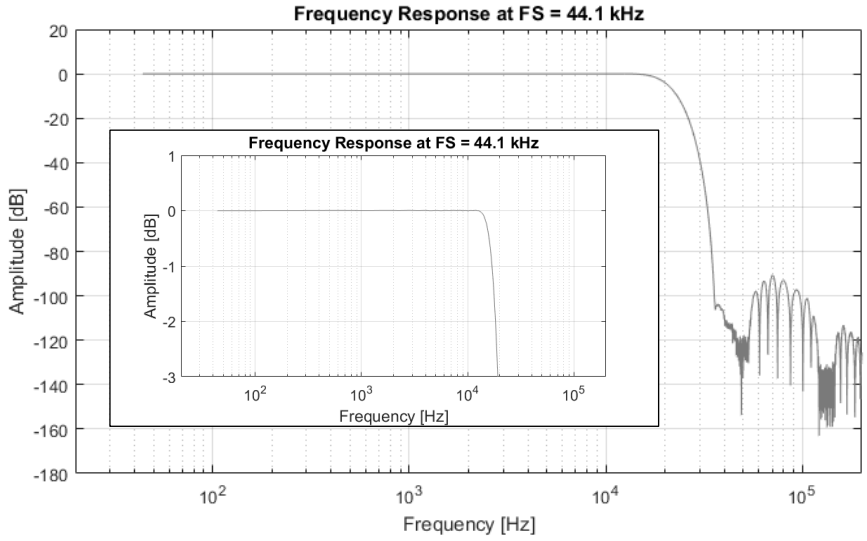
PCM Filter Frequency Response

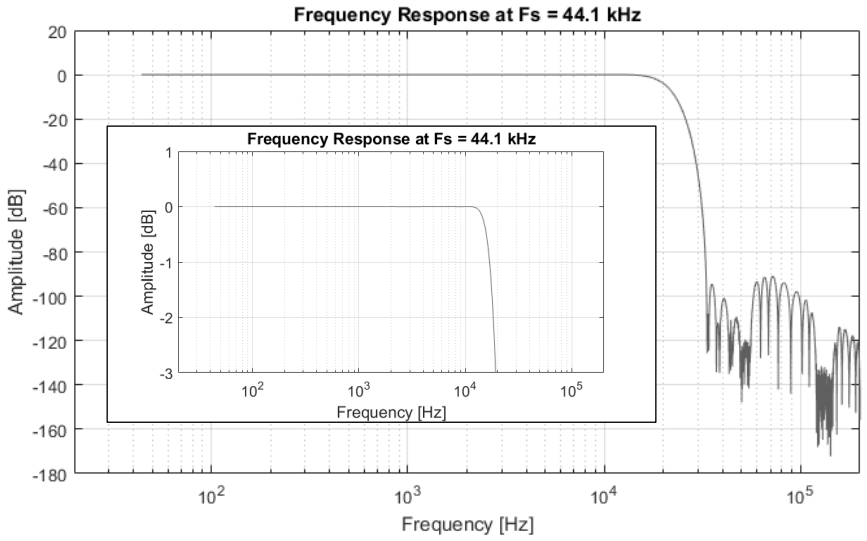
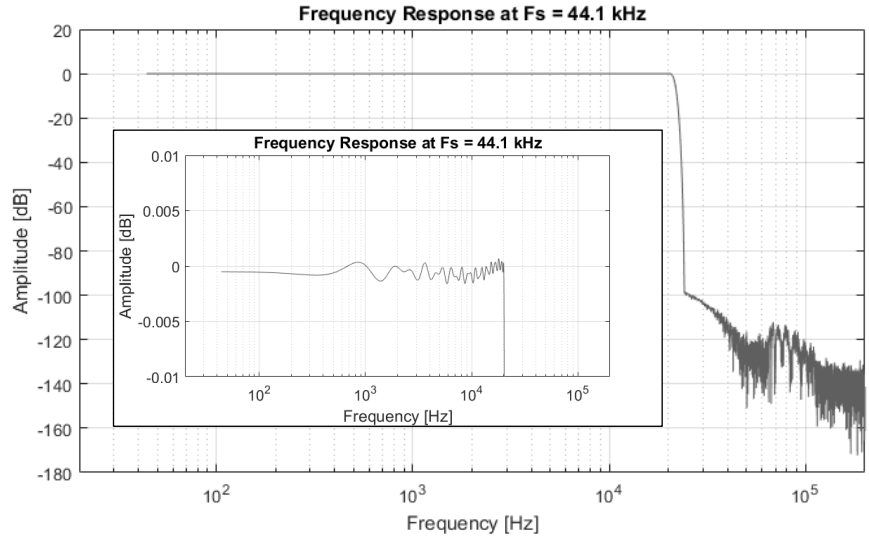
The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

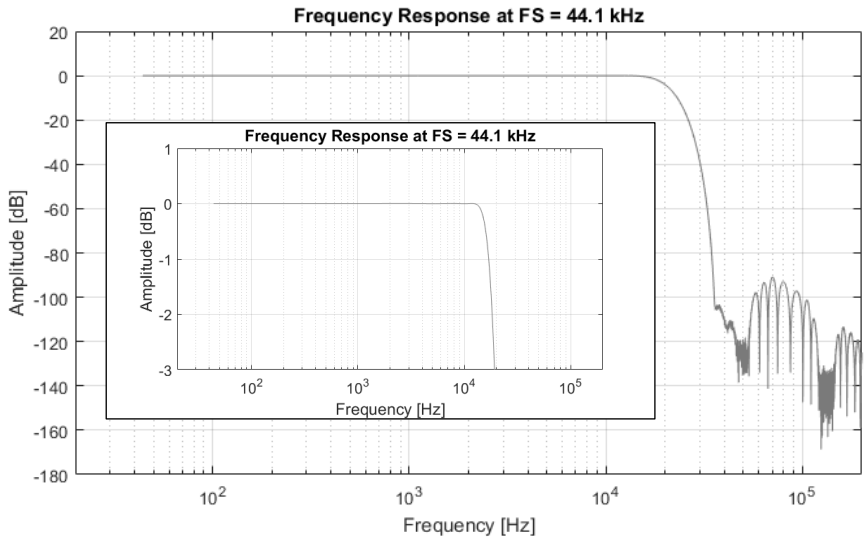
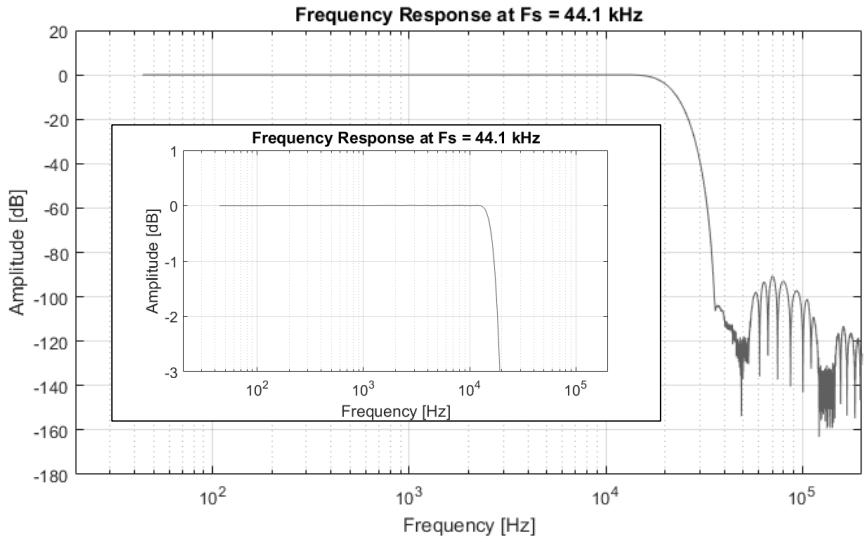
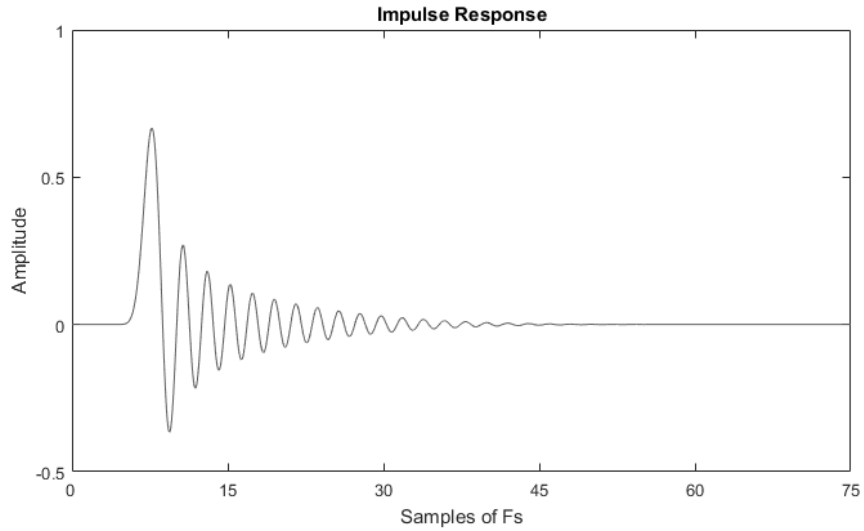
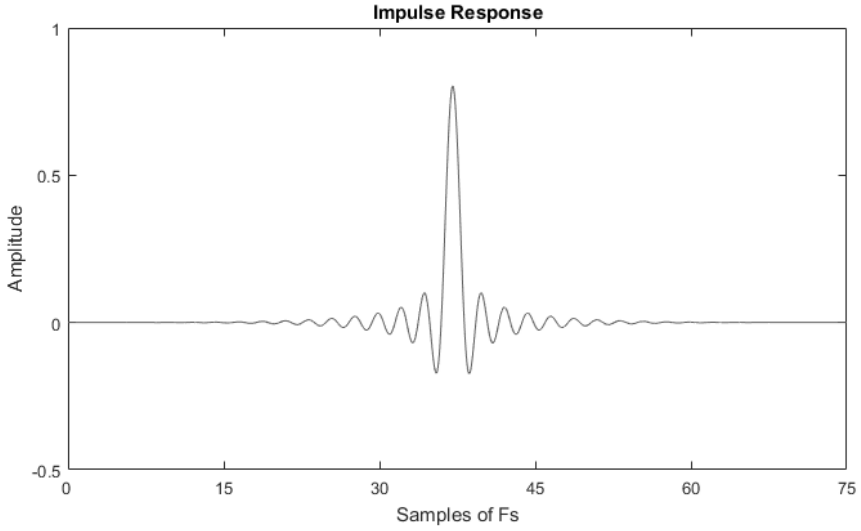
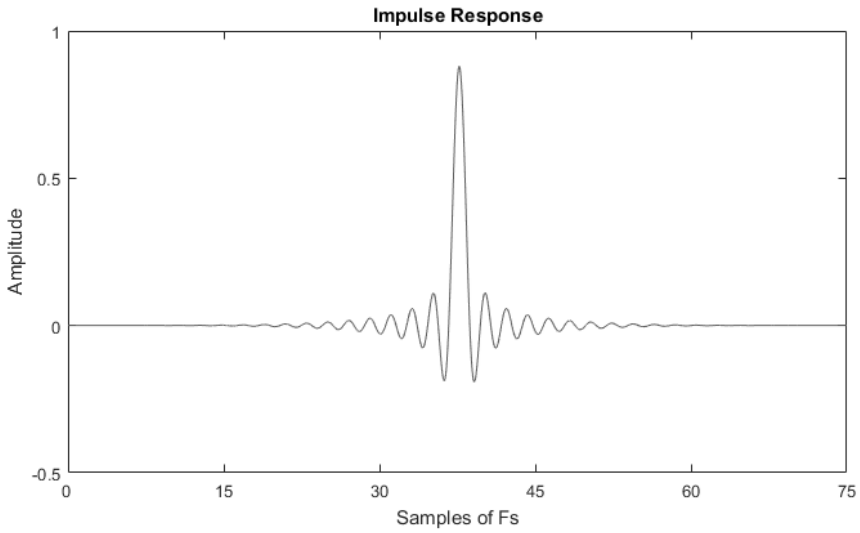
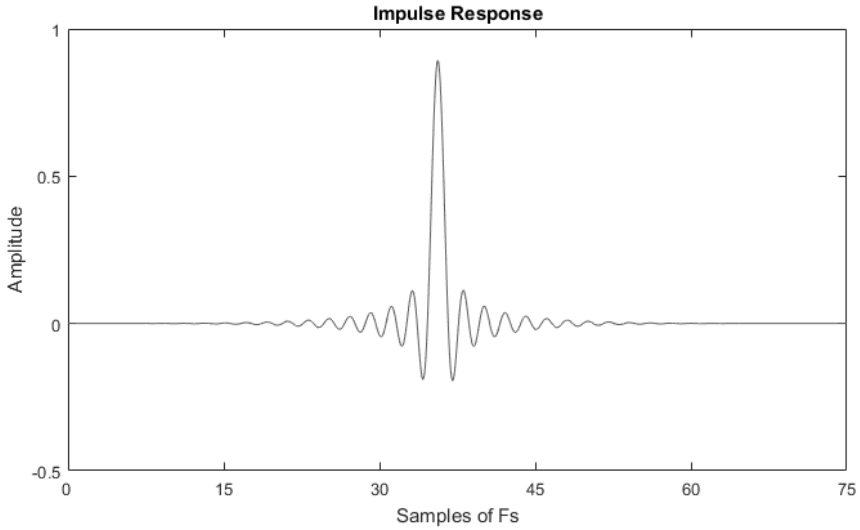
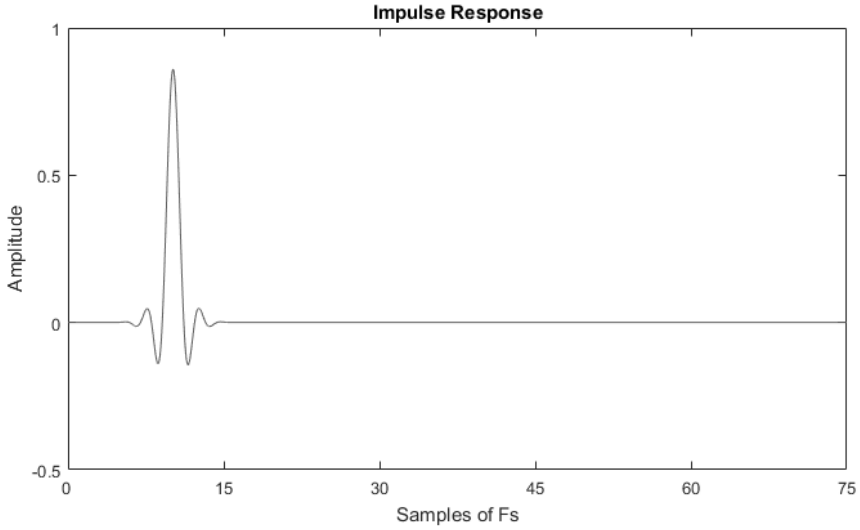
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 20 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from external impulse response. The extra sample delay to get the data encoded accounts for the external processing time to serialize the data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	
Linear Phase Slow Roll-Off	

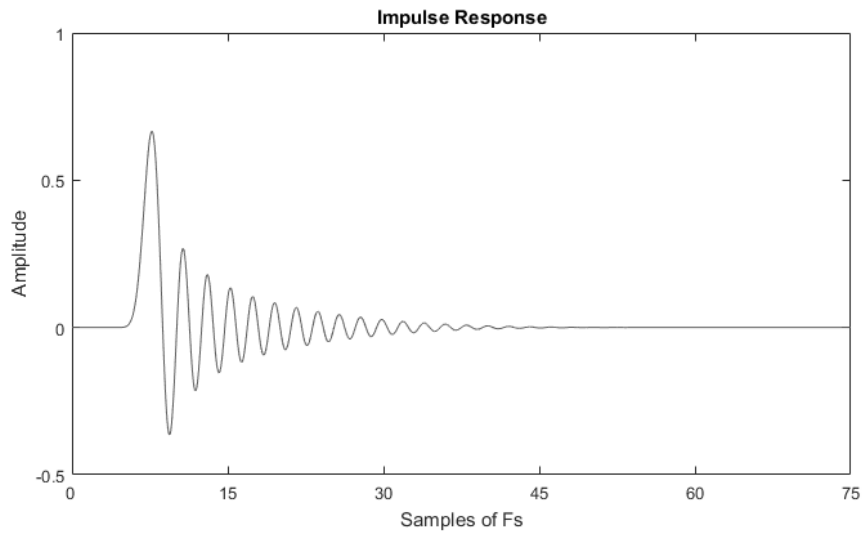
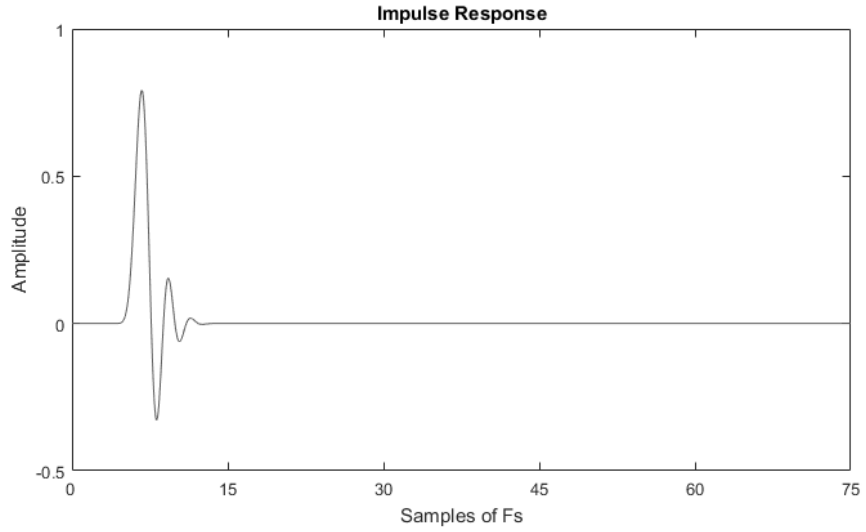
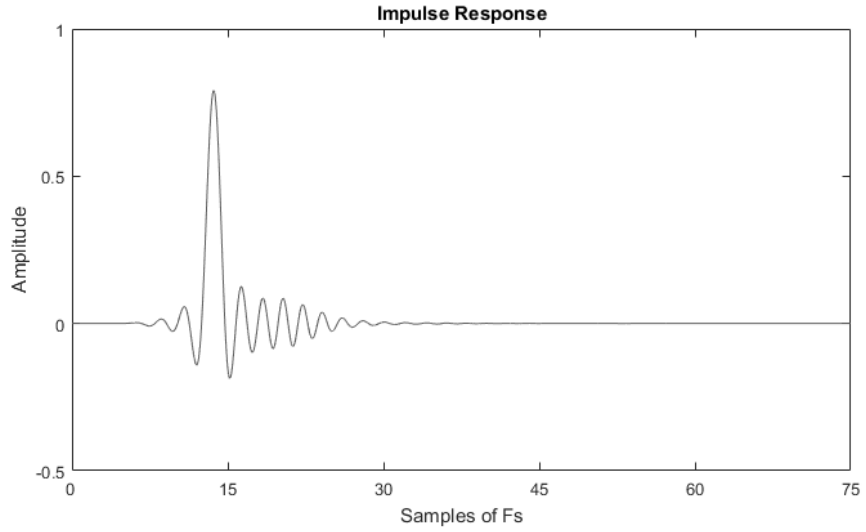
Minimum Phase Fast Roll-Off	
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 21 - PCM Filter Impulse Response

64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9039Q2M to be running in 64FS Mode. 64FS Mode can be manually entered by setting ENABLE_64FS_MODE to 1'b1, overriding the AUTO_FS_DETECT logic.

If using automatic sample rate detection with AUTO_FS_DETECT, 64FS Mode can be automatically accessed, unless AUTO_FS_DETECT_BLOCK_64FS is set to 1'b1.

Software Registers

- Register 0[6] ENABLE_64FS_MODE
  - Use for 64FS ratios, including 705.6/768kHz sample rates
- Register 3[7] AUTO_FS_DETECT
  - 1'b0: Manually set sample rate with Register 1[6:0]
  - 1'b1: Automatically determine the sample rate (default)
- Register 5[0] AUTO_FS_DETECT_BLOCK_64FS
  - 1'b0: Allows AUTO_FS_DETECT to enter 64FS Mode (default)
  - 1'b1: Blocks AUTO_FS_DETECT from entering 64FS mode

This mode enables the Minimum Phase 64FS filter. See filter properties.

Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is scaled at 768kHz. The measurement was taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase Double Rate	8us

Table 22 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.45FS	Hz
Stop band	-61dB	0.68FS			Hz
Group Delay		1.55/FS		2.35/FS	s
Flatness (ripple)					dB

Table 23 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz.

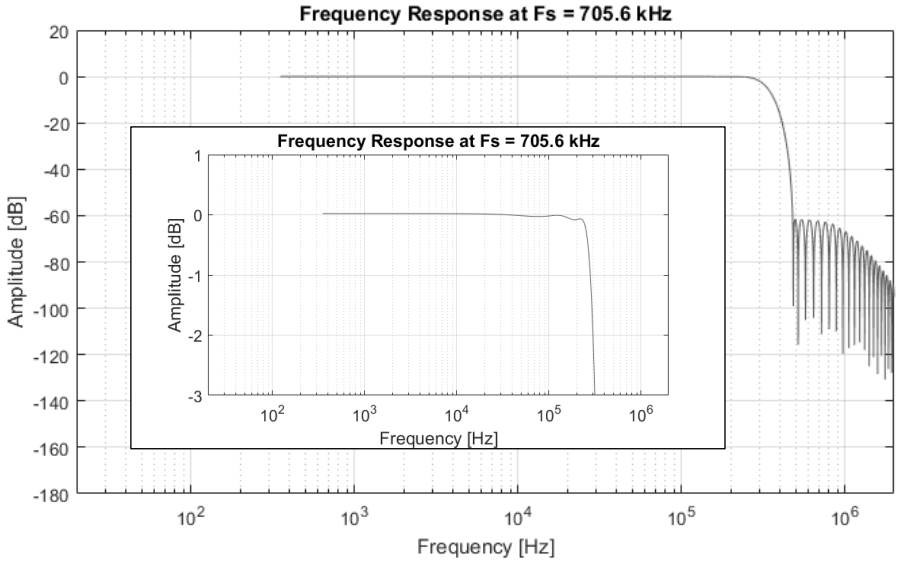


Figure 15 - Minimum Phase 64FS Frequency Response

Minimum Phase 64FS Impulse Response

The following impulse response was obtained from software simulations. It was measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream.

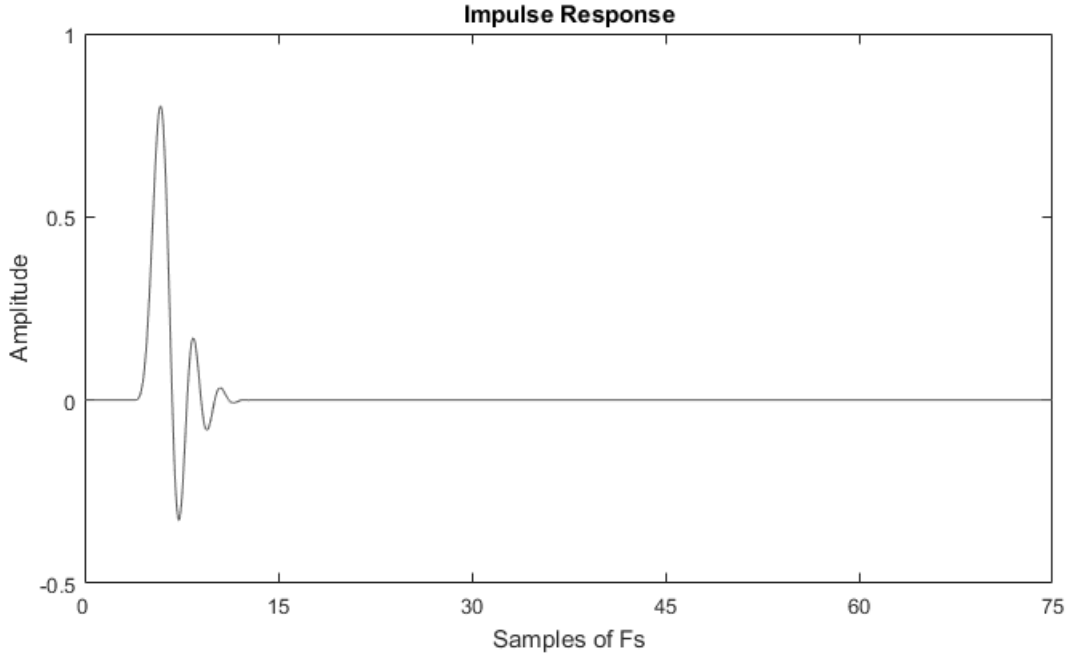


Figure 16 - Minimum Phase 64FS Impulse Response

Analog Features

Calibration Resistor

The ES9039Q2M features a ~50kΩ integrated resistor that is used for calibration of DAC voltage supplies AVCC_DAC1 and AVCC_DAC2. This calibration is required to maintain output level from device to device with the process varying DAC output impedance. The calibration resistor is accessible through GPIO8 (Pin 28) and terminated to ground as shown in the below figure.

To calibrate the AVCC_DAC1 and AVCC_DAC2 voltage supplies, a circuit is required to generate the voltage supply based on the resistor value. This can be done by generating a constant current and using that current through the internal calibration resistor to generate the reference voltage. This voltage is then buffered for the AVCC_DACx supply.

The ultra low noise ESS ES9312 voltage regulator features a calibration mode that can be paired with the ES9039Q2M AVCC_DAC1 and AVCC_DAC2 supplies. The ES9312 connects to the ES9039Q2M integrated calibration resistor, on GPIO8, and adjusts the DAC output supplies to maintain a tighter distribution on the output level. See Recommended Power Supply for connections.

By default, the switch is closed (CAL_RES_ENB = 1'b0), Register 42[7] = 1'b0 (input disabled), and Register 41[7] GPIO8_OE = 1'b0 (tristated).

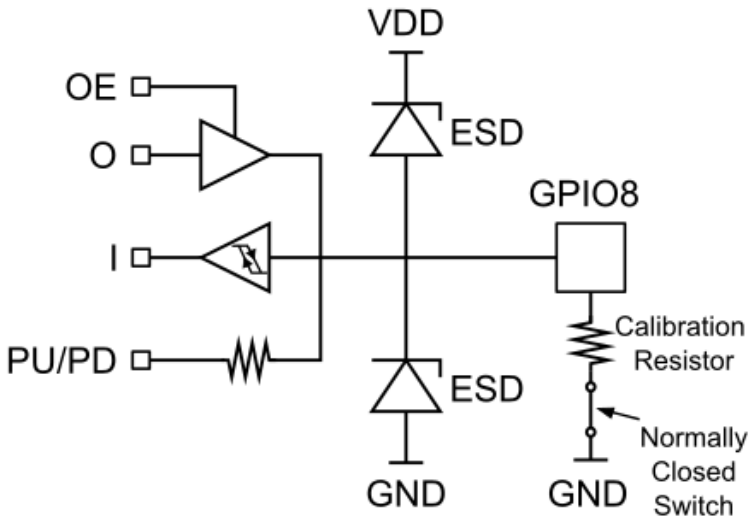


Figure 17 - GPIO8 Digital I/O with Calibration Resistor

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_DAC1 • AVCC_DAC2 • AVDD • VCCA • DVDD	 • +3.7V with respect to Ground • +3.7 V with respect to Ground • +3.7 V with respect to Ground • +3.7 V with respect to Ground • +1.4 V with respect to Ground
Storage Temperature	-65ºC to +150ºC
Operating Junction temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD(nom)+0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 24 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

I/O Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-Level Input Voltage	VIH	(AVDD / 2) + 0.4		V
Low-Level Input Voltage	VIL		0.4	V
High-Level Output Voltage	VOH	AVDD - 0.2		V
Low-Level Output Voltage	VOL		0.2	V

Table 25 - I/O Electrical Characteristics

Recommended Operating Conditions

These are the recommended operating conditions for the ES9039Q2M.

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20ºC to +85 ºC
AVCC_DAC1		3.3V
AVCC_DAC2		3.3V
AVDD		3.3V
VCCA		3.3V
DVDD	Internal	1.2V

Table 26 - Recommended Operating Conditions

Note: Supplied power is required to be within ±5% of the recommended condition.

Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)
T_A=25ºC, AVCC_R=AVCC_L=VCCA=AVDD=+3.3V, DVDD=+1.2V, fs=48kHz, DAC enabled, 1kHz sine full scale.

Parameter		Min	Typ.	Max	Unit
Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)					
AVCC_DAC1			5.9		mA
AVCC_DAC2			5.9		mA
VCCA			0.4		mA
AVDD			4.0		mA
Power Consumption			54		mW
Hardware Mode: 2 (Master mode with MCLK = 24.576MHz, FS=MCLK/512)					
AVCC_DAC1			6.8		mA
AVCC_DAC2			6.8		mA
VCCA			0.5		mA
AVDD			9.4		mA
Power Consumption			78		mW
Hardware Mode: 1 (Master mode with MCLK = 12.288MHz, FS=MCLK/256)					
AVCC_DAC1			6.2		mA
AVCC_DAC2			6.2		mA
VCCA			0.22		mA
AVDD			6.9		mA
Power Consumption			64		mW

Table 27 - Power Consumption with Test Conditions 1

Test Conditions 2 (unless otherwise noted)
T_A=25ºC, AVCC_R=AVCC_L=VCCA=AVDD=+3.3V, DVDD=+1.2V, fs=48kHz, DAC enabled, streaming zeros, automute enabled.

Parameter		Min	Typ.	Max	Unit
Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)					
AVCC_DAC1			0.8		mA
AVCC_DAC2			0.8		mA
VCCA			0.4		mA
AVDD			2.4		mA
Power Consumption			15		mW
Hardware Mode: 2 (Master mode with MCLK = 24.576MHz, FS=MCLK/512)					
AVCC_DAC1			1.5		mA
AVCC_DAC2			1.5		mA
VCCA			0.44		mA
AVDD			6.9		mA
Power Consumption			34		mW
Hardware Mode: 1 (Master mode with MCLK = 12.288MHz, FS=MCLK/256)					
AVCC_DAC1			1.0		mA
AVCC_DAC2			1.0		mA
VCCA			0.2		mA
AVDD			5.0		mA
Power Consumption			24		mW

Table 28 - Power Consumption with Test Conditions 2

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25°C, AVCC_DAC1 = AVCC_DAC2 = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, HW mode (I²S Master Mode)

Note: Performance numbers were measured using the ESS ES9039Q2M evaluation board v1.0, 10Vrms = 0dBFS input.

Parameter		Min	Typ.	Max	Unit
Resolution			32		Bit
Max MCLK Frequency				50	MHz
THD+N Ratio / THD Ratio @ fs=48kHz (differential)	0dBFS, BW=20Hz-20kHz		-120/-126		dB
THD+N Ratio / THD Ratio @ fs=96kHz (differential)	0dBFS, BW=20Hz-40kHz		-117/-126		dB
THD+N Ratio / THD Ratio @ fs=192kHz (differential)	0dBFS, BW=20Hz-80kHz		-114/-126		dB
THD+N Ratio / THD Ratio @ fs=384kHz (differential)	0dBFS, BW=20Hz-160kHz		-108/-126		dB
DNR (A-weighted) (2 Channel mode - Single Channel Diff)	-60dBFS		130		dB
DNR (A-weighted) (Mono mode - 2 Channel Sum Diff)			133		dB
Voltage Output Amplitude	Full-Scale Out		$0.889 * AVCC$		Vpp
Voltage Output Offset	Bipolar Zero Out		$\frac{AVCC}{2}$		V
Current Output Amplitude	Full-Scale Out		$\frac{1000 * 0.889 * AVCC}{Rdac}$		mApp
Current Output Offset	Bipolar Zero Out		$\frac{1000 * \left(\frac{AVCC}{2} - Vg\right)}{Rdac}$		mA
Output Impedance (Per + or - pin of each DAC output)	R_{DAC}		390 ± 15%		Ω

Table 29 - Performance Data

Timing Requirements

I²C Slave Interface Timing

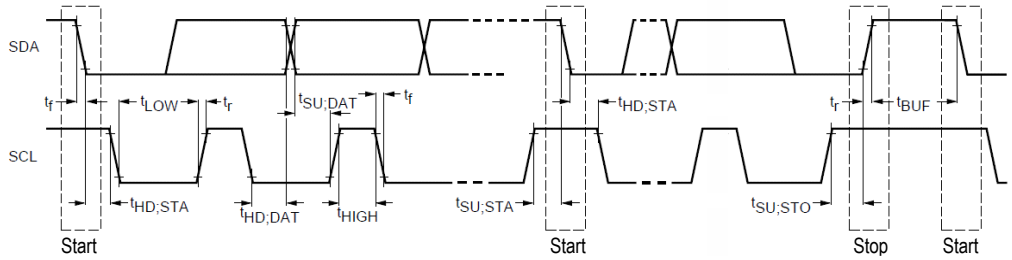


Figure 18 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 30 - I²C Slave Interface Timing Definitions

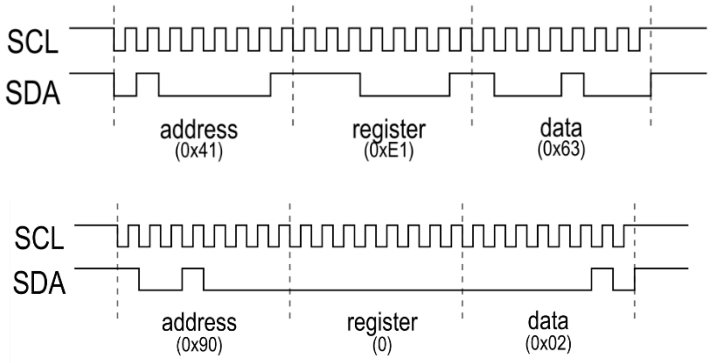


Figure 19 - I²C Single Byte Examples of Read and Write Instructions

SPI Slave Interface

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data.

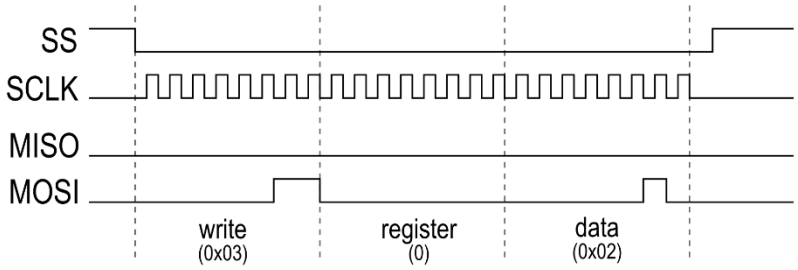


Figure 20 - SPI Single Byte Write

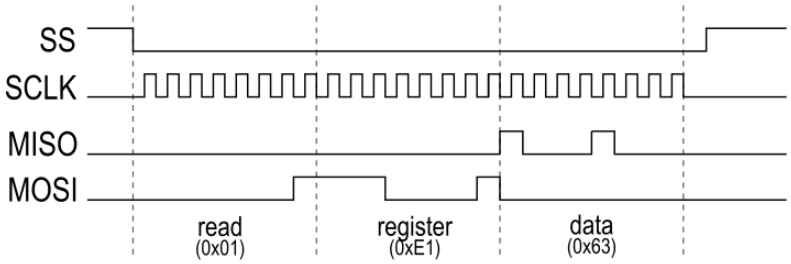


Figure 21 - SPI Single Byte Read

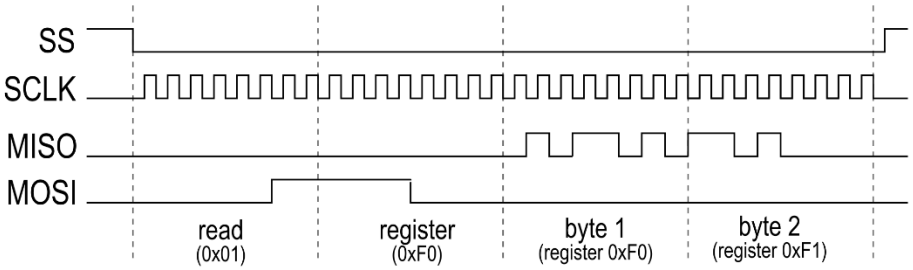


Figure 22 - SPI Multi-Byte Read

Audio Interface Timing

Audio data on DATA1-2 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK.

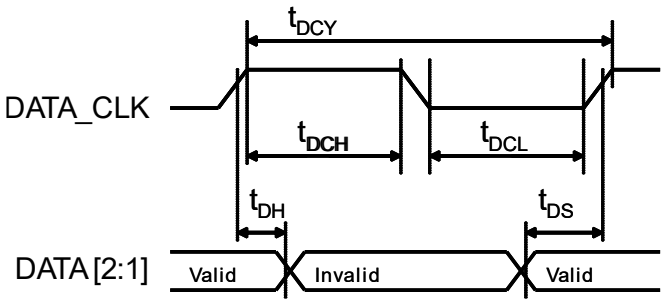


Figure 23 - Audio Interface Timing

Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATAx set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATAx hold time to DATA_CLK rising edge	t_{DH}	2.0		ns

Table 31 - Audio Interface Timing Definitions

Register Overview

The ES9039Q2M contains read/write and read-only registers. A system clock must be present to access registers.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-byte register must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Read/Write Register Addresses

Register 0 - 142 (0x00 - 0x8E) are read/write registers.

Read-Only Register Addresses

Register 224 - 251 (0xE0 - 0xFB) are read only registers.

Multi-Byte Registers

Multi-byte register must be written from LSB to MSB. Data is latched when MSB is written.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_ MODE	RESERVED				DAC_MODE	RESERVED
0x01	1	SYS MODE CONFIG	ENABLE_DAC_ CLK	SYNC_MODE	RESERVED		ENABLE_SPDIF _DECODE	ENABLE_DOP_ DECODE	ENABLE_DSD_ DECODE	ENABLE_TDM_ DECODE
0x02	2	RESERVED	RESERVED							
0x03	3	DAC CLOCK CONFIG	AUTO_FS_DET ECT	SELECT_IDAC_ HALF	SELECT_IDAC_NUM					
0x04	4	CLOCK CONFIG	MASTER_BCK_DIV							
0x05	5	CLK GEAR SELECT	RESERVED		SEL_CLK_GEAR		RESERVED	AUTO_CLK_ GEAR	RESERVED	AUTO_FS_ DETECT_ BLOCK_64FS
0x06-0x09	6-9	RESERVED	RESERVED							
0x0A	10	INTERUPT MASKP	BCK_WS_FAIL_ MASKP	DOP_VALID_ MASKP	SS_FULL_ RAMP_CH2_ MASKP	SS_FULL_ RAMP_CH1_ MASKP	AUTOMUTE_ FLAG_CH2_ MASKP	AUTOMUTE_ FLAG_CH1_ MASKP	VOL_MIN_CH2_ MASKP	VOL_MIN_CH1_ MASKP
0x0B	11		RESERVED		INPUT_SELECT_OVERRIDE_MASKP		TDM_VALID_ EDGE_MASKP	RESERVED		
0x0C-0x0E	12-14	RESERVED	RESERVED							
0x0F	15	INTERUPT MASKN	BCK_WS_FAIL_ MASKN	DOP_VALID_ MASKN	SS_FULL_ RAMP_CH2_ MASKN	SS_FULL_ RAMP_CH1_ MASKN	AUTOMUTE_ FLAG_CH2_ MASKN	AUTOMUTE_ FLAG_CH1_ MASKN	VOL_MIN_CH2_ MASKN	VOL_MIN_CH1_ MASKN
0x10	16		RESERVED		INPUT_SELECT_OVERRIDE_MASKN		TDM_VALID_ EDGE_MASKN	RESERVED		
0x11-0x13	17-19	RESERVED	RESERVED							
0x14	20	INTERRUPT CLEAR	BCK_WS_FAIL_ CLEAR	DOP_VALID_ CLEAR	SS_FULL_ RAMP_CH2_ CLEAR	SS_FULL_ RAMP_CH1_ CLEAR	AUTOMUTE_ FLAG_CH2_ CLEAR	AUTOMUTE_ FLAG_CH1_ CLEAR	VOL_MIN_CH2_ CLEAR	VOL_MIN_CH1_ CLEAR
0x15	21		RESERVED		INPUT_SELECT_OVERRIDE_CLEAR		TDM_VALID_ EDGE_CLEAR	RESERVED		
0x16-0x1C	22-28	RESERVED	RESERVED							
0x1D	29	DPLL BW	DPLL_BW				RESERVED			
0x1E-0x21	30-33	RESERVED	RESERVED							
0x22	34	DATA PATH CONFIG	MONO_MODE	CAL_RES_ENB	RESERVED					
0x23	35	PCM 4X GAIN	RESERVED						CH2_PCM_4X_ GAIN	CH1_PCM_4X_ GAIN
0x24	36	RESERVED	RESERVED							
0x25	37	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x26	38	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x27	39	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x28	40	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x29	41	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x2A	42	GPIO INPUT	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x2B	43	GPIO WK EN	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x2C	44	INVERT GPIO	INVERT_GPIO8	INVERT_GPIO7	INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1
0x2D	45	GPIO READ	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x2E	46	GPIO OUTPUT LOGIC	RESERVED	GPIO_SEL	GPIO_OR_SS_ RAMP	GPIO_OR_VOL_ MIN	GPIO_OR_ AUTOMUTE	GPIO_AND_SS_ RAMP	GPIO_AND_VOL _MIN	GPIO_AND_ AUTOMUTE
0x2F	47		GPIO_DAC_ MODE	RESERVED						
0x30	48	PWM1 COUNT	PWM1_COUNT							
0x31	49	PWM1 FREQUENCY	PWM1_FREQ							
0x32	50		PWM1_FREQ							
0x33	51	PWM2 COUNT	PWM2_COUNT							
0x34	52	PWM2 FREQUENCY	PWM2_FREQ							
0x35	53		PWM2_FREQ							
0x36	54	PWM3 COUNT	PWM3_COUNT							
0x37	55	PWM3 FREQUENCY	PWM3_FREQ							
0x38	56		PWM3_FREQ							
0x39	57	INPUT SELECTION	AUTO_CH_ DETECT	ENABLE_DSD_ FAULT_ DETECTION	DSD_MASTER_ MODE	PCM_MASTER_ MODE	RESERVED	INPUT_SEL		AUTO_INPUT_ SEL
0x3A	58	MASTER ENCODER CONFIG	TDM_RESYNC	BCK_INV	RESERVED	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_WS_ INVERT	MASTER_BCK_ INVERT
0x3B	59	TDM CONFIG	RESERVED			TDM_CH_NUM				
0x3C	60	TDM CONFIG1	TDM_LJ_MODE	TDM_VALID_ EDGE	TDM_DAISY_ CHAIN	RESERVED				
0x3D	61	TDM CONFIG2	RESERVED	TDM_BIT_WIDTH		TDM_DATA_LATCH_ADJ				
0x3E	62	BCK/WS MONITOR CONFIG	DISABLE_DSD_ DC	DISABLE_DSD_ MUTE	ENABLE_WS_ MONITOR	ENABLE_BCK_ MONITOR	DISABLE_PCM_ DC	RESERVED		
0x3F	63	RESERVED	RESERVED							
0x40	64	CH1 SLOT CONFIG	DSD_CH1_SOURCE			TDM_CH1_SLOT_SEL				
0x41	65	CH2 SLOT CONFIG	DSD_CH2_SOURCE			TDM_CH2_SLOT_SEL				
0x42-0x49	66-73	RESERVED	RESERVED							
0x4A	74	VOLUME CH1	VOLUME_CH1							
0x4B	75	VOLUME CH2	VOLUME_CH2							
0x4C-0x51	76-81	RESERVED	RESERVED							
0x52	82	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x53	83	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x54	84	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x55	85	RESERVED	RESERVED							
0x56	86	DAC MUTE	RESERVED						DAC_MUTE_ CH2	DAC_MUTE_ CH1

0x57	87	DAC INVERT	RESERVED					DAC_INVERT_CH2	DAC_INVERT_CH1
0x58	88	FILTER SHAPE	RESERVED				FILTER_SHAPE		
0x59	89	IIR BANDWIDTH & S/PDIF SEL	SPDIF_SEL			VOLUME_HOLD	IIR_BW		
0x5A	90	DAC PATH CONFIG	RESERVED				BYPASS_IIR	BYPASS_FIR4X	BYPASS_FIR2X
0x5B	91	THD C2	THD_C2_CH1						
0x5C	92		THD_C2_CH1						
0x5D	93		THD_C2_CH2						
0x5E	94		THD_C2_CH2						
0x5F-0x6A	95-106	RESERVED	RESERVED						
0x6B	107	THD C3	THD_C3_CH1						
0x6C	108		THD_C3_CH1						
0x6D	109		THD_C3_CH2						
0x6E	110		THD_C3_CH2						
0x6F-0x7A	111-122	RESERVED	RESERVED						
0x7B	123	AUTOMUTE ENABLE	RESERVED					AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x7C	124	AUTOMUTE TIME	AUTOMUTE_TIME						
0x7D	125		RESERVED			MUTE_RAMP_TO_GROUND	AUTOMUTE_TIME		
0x7E	126	AUTOMUTE LEVEL	AUTOMUTE_LEVEL						
0x7F	127		AUTOMUTE_LEVEL						
0x80	128	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL						
0x81	129		AUTOMUTE_OFF_LEVEL						
0x82	130	SOFT RAMP CONFIG	RESERVED			SOFT_RAMP_TIME			
0x83-0x86	131-134	RESERVED	RESERVED						
0x87	135	PROGRAM RAM CONTROL	SPDIF_LOAD_USER_BITS	RESERVED				PROG_COEFF_WE	PROG_COEFF_EN
0x88	136	S/PDIF READ CONTROL	RESERVED			SPDIF_DATA_SEL			
0x89	137	PROGRAM RAM ADDRESS	PROG_COEFF_STAGE	PROG_COEFF_ADDR					
0x8A	138	PROGRAM RAM DATA	PROG_COEFF_IN						
0x8B	139		PROG_COEFF_IN						
0x8C	140		PROG_COEFF_IN						
0x8D-0x91	141-145	RESERVED	RESERVED						
0xE0	224	RESERVED	RESERVED						
0xE1	225	CHIP ID READ	CHIP_ID						
0xE2-0xE4	226	RESERVED	RESERVED						
0xE5	229	INTERRUPT STATES	BCK_WS_FAIL_STATE	DOP_VALID_STATE	SS_FULL_RAMP_STATE		AUTOMUTE_STATE		VOL_MIN_STATE
0xE6	230		RESERVED		INPUT_SELECT_OVERRIDE_STATE		TDM_DATA_VALID_STATE	RESERVED	
0xE7-0xE9	231-233	RESERVED	RESERVED						
0xEA	234	INTERRUPT SOURCES	BCK_WS_FAIL_SOURCE	DOP_VALID_SOURCE	SS_FULL_RAMP_SOURCE		AUTOMUTE_SOURCE		VOL_MIN_SOURCE
0xEB	235		RESERVED		INPUT_SELECT_OVERRIDE_SOURCE		TDM_DATA_VALID_SOURCE	RESERVED	
0xEC-0xEF	236-239	RESERVED	RESERVED						
0xF0	240	GPIO READBACK	GPIO8_I_READ	GPIO7_I_READ	GPIO6_I_READ	GPIO5_I_READ	GPIO4_I_READ	GPIO3_I_READ	GPIO2_I_READ	GPIO1_I_READ
0xF1	241	VOL MIN READ	RESERVED						VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242	AUTOMUTE READ	RESERVED						AUTOMUTE_CH2	AUTOMUTE_CH1
0xF3	243	SOFT RAMP UP READ	RESERVED						SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xF4	244	SOFT RAMP DOWN READ	RESERVED						SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xF5	245	INPUT STREAM READBACK	RESERVED			SPDIF_VALID	TDM_DATA_VALID	DOP_VALID	INPUT_SELECT_OVERRIDE	
0xF6	246	PROG COEFF OUT READ	PROG_COEFF_OUT							
0xF7	247		PROG_COEFF_OUT							
0xF8	248		PROG_COEFF_OUT							
0xF9-0xFA	249-250	RESERVED	RESERVED							
0xFB	251	S/PDIF DATA READ	SPDIF_DATA_READ							

Table 32 - Register Map

Register Listing

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5:2]	[1]	[0]
Default	1'b0	1'b0	4'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core. • 1'b0: Normal operation • 1'b1: Reset digital core (all settings are set to default)
[6]	ENABLE_64FS_MODE	Enables 64FS mode to run the DAC interpolation path at 64FS. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled Note: This mode is used only for PCM high sample rates such as 768kHz with a 49.152MHz or 384kHz with 24.576MHz clock
[5:2]	RESERVED	N/A
[1]	DAC_MODE	Enables the analog section of the DAC. • 1'b0: DAC disabled (default) • 1'b1: DAC enabled
[0]	RESERVED	N/A

Register 1: SYS MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b0	2'b11	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_DAC_CLK	Enables DAC interpolation path clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[6]	SYNC_MODE	Enables SYNC mode. • 1'b0: ASYNC mode enabled (default) • 1'b1: SYNC mode enabled
[5:4]	RESERVED	N/A
[3]	ENABLE_SPDIF_DECODE	Enables S/PDIF decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 2: RESERVED

Register 3: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	Automatically determine optimal (SYS_CLK/CLK_IDAC ratio) according to detected FS. • 1'b0: Disabled, use reg 3[5:0] SELECT_IDAC_NUM to set ratio. • 1'b1: Enabled, overrides reg 3[5:0] SELECT_IDAC_NUM (default) Note: Cannot be used in ASYNC mode.
[6]	SELECT_IDAC_HALF	• 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 4: CLOCK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value).

Register 5: CLK GEAR SELECT

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'b00	2'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:4]	SEL_CLK_GEAR	MCLK clock gearing, outputs SYS_CLK to the rest of the device. • 2'd0: SYS_CLK = MCLK/1 • 2'd1: SYS_CLK = MCLK/2 • 2'd2: SYS_CLK = MCLK/4 • 2'd3: SYS_CLK = MCLK/8
[3]	RESERVED	N/A
[2]	AUTO_CLK_GEAR	Enable automatic clock gearing. In automatic clock gearing, MCLK will be geared down until 128FS ≤ SYS_CLK < 256FS. • 1'b0: Disabled, SYS_CLK = SEL_CLK_GEAR (default) • 1'b1: Enabled, SYS_CLK will decrease by up to SEL_CLK_GEAR • 1'b1: Enabled, SYS_CLK will decrease by up to SEL_CLK_GEAR
[1]	RESERVED	N/A
[0]	AUTO_FS_DETECT_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected SYS_CLK/CLK_IDAC ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 9-6: RESERVED

Register 11-10: INTERUPT MASKP

Bits	[15:14]	[13:12]	[11]	[10:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	3'b000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:12]	INPUT_SELECT_OVERRIDE_MASKP	Masks negative to positive interrupt transitions. • 2'b00: Ignore interrupt (default) • 2'b11: Service interrupt if flag transitions from negative to positive
[11]	TDM_VALID_EDGE_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[10:8]	RESERVED	N/A
[7]	BCK_WS_FAIL_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[6]	DOP_VALID_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[5]	SS_FULL_RAMP_CH2_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[4]	SS_FULL_RAMP_CH1_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[3]	AUTOMUTE_FLAG_CH2_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[2]	AUTOMUTE_FLAG_CH1_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from negative to positive

Register 14-12: RESERVED

Register 16-15: INTERUPT MASKN

Bits	[15:14]	[13:12]	[11]	[10:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	3'b000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:12]	INPUT_SELECT_OVERRIDE_MASKN	Masks positive to negative interrupt transitions. • 2'b00: Ignore interrupt (default) • 2'b11: Service interrupt if flag transitions from positive to negative
[11]	TDM_VALID_EDGE_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[10:8]	RESERVED	N/A
[7]	BCK_WS_FAIL_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[6]	DOP_VALID_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if toggled from positive to negative
[5]	SS_FULL_RAMP_CH2_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[4]	SS_FULL_RAMP_CH1_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[3]	AUTOMUTE_FLAG_CH2_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[2]	AUTOMUTE_FLAG_CH1_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt transitions. • 1'b0: Ignore interrupt (default) • 1'b1: Service interrupt if flag transitions from positive to negative

Register 19-17: RESERVED

Register 21-20: INTERRUPT CLEAR

Bits	[15:14]	[13:12]	[11]	[10:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	3'b000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:12]	INPUT_SELECT_OVERRIDE_CLEAR	Toggle high-low to clear and re-arm interrupt.
[11]	TDM_VALID_EDGE_CLEAR	Toggle high-low to clear and re-arm interrupt.
[10:8]	RESERVED	N/A
[7]	BCK_WS_FAIL_CLEAR	Toggle high-low to clear and re-arm interrupt.
[6]	DOP_VALID_CLEAR	Toggle high-low to clear and re-arm interrupt.
[5]	SS_FULL_RAMP_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[4]	SS_FULL_RAMP_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.
[3]	AUTOMUTE_FLAG_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[2]	AUTOMUTE_FLAG_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.
[1]	VOL_MIN_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[0]	VOL_MIN_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.

Register 28-22: RESERVED

Register 29: DPLL BW

Bits	[7:4]	[3:0]
Default	4'd4	4'd0

Bits	Mnemonic	Description
[7:4]	DPLL_BW	Sets the bandwidth of the DPLL. 4'd0: Reserved 4'd1: Lowest Bandwidth 4'd15: Highest Bandwidth
[3:0]	RESERVED	N/A

Register 33-30: RESERVED

Register 34: DATA PATH CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'b000000

Bits	Mnemonic	Description
[7]	MONO_MODE	Enables MONO Mode Note: Does not turn off unused data path for power saving
[6]	CAL_RES_ENB	Selects the calibration resistor connection on GPIO8. • 1'b0: DAC calibration resistor enabled (default) • 1'b1: DAC calibration resistor disabled, normal GPIO
[5:0]	RESERVED	N/A

Register 35: PCM 4X GAIN

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	CH2_PCM_4X_GAIN	Changes the gain on the CH2 interpolation path after the IIR. • 1'b0: 1x gain • 1'b1: 4x gain Note: Not available in DSD mode.
[0]	CH1_PCM_4X_GAIN	Changes the gain on the CH1 interpolation path after the IIR. • 1'b0: 1x gain • 1'b1: 4x gain Note: Not available in DSD mode.

Register 36: RESERVED

GPIO Registers

Register 37: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd7	4'd13

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 • 4'd0: Analog shutdown - shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_BCK – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output (default) • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: Analog shutdown - shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLKEN_1FS – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output (default) • 4'd14: Soft ramp done – output • 4'd15: Reserved

Register 38: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO3_CFG	Configures GPIO3 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: SYS_CLK – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved

Register 39: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_BCK – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO5_CFG	Configures GPIO5 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLKEN_1FS – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved

Register 40: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configures GPIO8 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved
[3:0]	GPIO7_CFG	Configures GPIO7 • 4'd0: Analog shutdown - shutdown (default) • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: SYS_CLK – output • 4'd4: Interrupt – output • 4'd5: Mute all channels – input • 4'd6: System mode control – input • 4'd7: Lock status – output • 4'd8: Reserved • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Minimum volume – output • 4'd13: Automute status – output • 4'd14: Soft ramp done – output • 4'd15: Reserved

Register 41: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1

Bits	Mnemonic	Description
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 (default) • 1'b1: GPIO8 Output enabled
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 (default) • 1'b1: GPIO7 Output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 • 1'b1: GPIO2 Output enabled (default)
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 • 1'b1: GPIO1 Output enabled (default)

Register 42: GPIO INPUT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_SDB	• 1'b0: Disables GPIO8 input (default) • 1'b1: Enables GPIO8 input
[6]	GPIO7_SDB	• 1'b0: Disables GPIO7 input (default) • 1'b1: Enables GPIO7 input
[5]	GPIO6_SDB	• 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_SDB	• 1'b0: Disables GPIO5 input (default) • 1'b1: Enables GPIO5 input
[3]	GPIO4_SDB	• 1'b0: Disables GPIO4 input (default) • 1'b1: Enables GPIO4 input
[2]	GPIO3_SDB	• 1'b0: Disables GPIO3 input (default) • 1'b1: Enables GPIO3 input
[1]	GPIO2_SDB	• 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_SDB	• 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input

Register 43: GPIO WK EN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 44: INVERT GPIO

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INVERT_GPIO8	• 1'b1: Inverts GPIO8 output.
[6]	INVERT_GPIO7	• 1'b1: Inverts GPIO7 output.
[5]	INVERT_GPIO6	• 1'b1: Inverts GPIO6 output.
[4]	INVERT_GPIO5	• 1'b1: Inverts GPIO5 output.
[3]	INVERT_GPIO4	• 1'b1: Inverts GPIO4 output.
[2]	INVERT_GPIO3	• 1'b1: Inverts GPIO3 output.
[1]	INVERT_GPIO2	• 1'b1: Inverts GPIO2 output.
[0]	INVERT_GPIO1	• 1'b1: Inverts GPIO1 output.

Register 45: GPIO READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_READ	• 1'b0: GPIO8 Readback disabled (default) • 1'b1: Allow readback of GPIO8_I Note: Requires corresponding GPIOx_SDB to be set.
[6]	GPIO7_READ	• 1'b0: GPIO7 Readback disabled (default) • 1'b1: Allow readback of GPIO7_I Note: Requires corresponding GPIOx_SDB to be set.
[5]	GPIO6_READ	• 1'b0: GPIO6 Readback disabled (default) • 1'b1: Allow readback of GPIO6_I Note: Requires corresponding GPIOx_SDB to be set.
[4]	GPIO5_READ	• 1'b0: GPIO5 Readback disabled (default) • 1'b1: Allow readback of GPIO5_I Note: Requires corresponding GPIOx_SDB to be set.
[3]	GPIO4_READ	• 1'b0: GPIO4 Readback disabled (default) • 1'b1: Allow readback of GPIO4_I Note: Requires corresponding GPIOx_SDB to be set.
[2]	GPIO3_READ	• 1'b0: GPIO3 Readback disabled (default) • 1'b1: Allow readback of GPIO3_I Note: Requires corresponding GPIOx_SDB to be set.
[1]	GPIO2_READ	• 1'b0: GPIO2 Readback disabled (default) • 1'b1: Allow readback of GPIO2_I Note: Requires corresponding GPIOx_SDB to be set.
[0]	GPIO1_READ	• 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I Note: Requires corresponding GPIOx_SDB to be set.

Register 47-46: GPIO OUTPUT LOGIC

Bits	[15]	[14:7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	8'd0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[15]	GPIO_DAC_MODE	When any GPIO_CFG is "System mode control": • 1'b0: Disable datapath when GPIO input is 1'b1 • 1'b1: Enable datapath when GPIO input is 1 When GPIOx input is 1'b0, system mode is determined by register 0[1] DAC_MODE.
[14:7]	RESERVED	N/A
[6]	GPIO_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2
[5]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(ss_full_ramp[CHx])
[4]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(automute[CHx])
[3]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(vol_min[CHx])
[2]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(ss_full_ramp[CHx]) (default) Note: Overridden by GPIO_OR_SS_RAMP.
[1]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(automute[CHx]) (default) Note: Overridden by GPIO_OR_AUTOMUTE.
[0]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(vol_min[CHx]) (default) Note: Overridden by GPIO_OR_VOL_MIN.

Register 48: PWM1 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 50-49: PWM1 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM1\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM1\_COUNT}}{\text{PWM1\_FREQ} + 1} \cdot 100$

Register 51: PWM2 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 53-52: PWM2 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM2\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM2\_COUNT}}{\text{PWM2\_FREQ} + 1} \cdot 100$

Register 54: PWM3 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 56-55: PWM3 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM3\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM3\_COUNT}}{\text{PWM3\_FREQ} + 1} \cdot 100$

DAC Registers

Register 57: INPUT SELECTION

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_FAULT_DETECTION	Sets a channel to a DSD mute pattern (0x96) if the DSD data has no changes in 64 DATA_CLKs. • 1'b0: Disabled • 1'b1: Enabled (default)
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	PCM_MASTER_MODE	PCM master mode config. • 1'b0: PCM slave mode (default) • 1'b1: PCM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	RESERVED	N/A
[2:1]	INPUT_SEL	Selects input data format when AUTO_INPUT_SEL is disabled. • 2'd0: PCM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: S/PDIF
[0]	AUTO_INPUT_SEL	Automatic input data selection config. • 1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default) • 1'b1: Automatically determine the input data format. Note: When using AUTO_INPUT_SEL & DSD, it is required that DSD data lines are on DATA1 & DATA2.

Register 58: MASTER ENCODER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. • 1'b0: Enable TDM decoder synchronization (default) • 1'b1: Force TDM decoder to desynchronize.
[6]	BCK_INV	Invert the slave BCK • 1'b0: Normal operation • 1'b1: Invert slave BCK
[5]	RESERVED	N/A
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32-bit (default) • 2'd1: 24-bit • 2'd2: 16-bit • 2'd3: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 59: TDM CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Total number of TDM slots per frame = TDM_CH_NUM + 1.

Register 60: TDM CONFIG1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd0

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I²S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5]	TDM_DAISY_CHAIN	TDM daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:0]	RESERVED	N/A

Register 61: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b1	2'b00	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	TDM_DATA_LATCH_ADJ	Sets the position of the start bit within each TDM slot. Can be moved by TDM_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Number of clock cycles to wait

Register 62: BCK/WS MONITOR CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DISABLE_DSD_DC	• 1'b0: DSD DC can trigger an automute if automute is enabled (default) • 1'b1: DSD DC is ignored.
[6]	DISABLE_DSD_MUTE	• 1'b0: DSD mute pattern can trigger an automute is automute is enabled (default) • 1'b1: DSD mute pattern is ignored.
[5]	ENABLE_WS_MONITOR	Enable WS monitor. • 1'b0: Disable • 1'b1: Enable (default)
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. • 1'b0: Disable • 1'b1: Enable (default)
[3]	DISABLE_PCM_DC	• 1'b0: PCM DC signal can trigger an automute if automute is enabled. (default) • 1'b1: PCM DC is ignored.
[2:0]	RESERVED	N/A

Register 63: RESERVED

Register 64: CH1 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	DSD_CH1_SOURCE	Selects the source for the CH1 DSD data. • 3'd0: DATA1 (default) • 3'd1: DATA2 • 3'd2: GPIO1 • 3'd3: GPIO2 • 3'd4: GPIO3 • 3'd5: GPIO4 • 3'd6: GPIO5 • 3'd7: GPIO6 Note: When using AUTO_INPUT_SEL & DSD, it is required that DSD data lines are on DATA1 & DATA2.
[4:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. Note: Valid for TDM, I²S and DoP.

Register 65: CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd1	5'd1

Bits	Mnemonic	Description
[7:5]	DSD_CH2_SOURCE	Selects the source for the CH2 DSD data. • 3'd0: DATA1 • 3'd1: DATA2 (default) • 3'd2: GPIO1 • 3'd3: GPIO2 • 3'd4: GPIO3 • 3'd5: GPIO4 • 3'd6: GPIO5 • 3'd7: GPIO6 Note: When using AUTO_INPUT_SEL & DSD, it is required that DSD data lines are on DATA1 & DATA2.
[4:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. Note: Valid for TDM, I²S and DoP.

Register 73-66: RESERVED

Register 74: VOLUME CH1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_CH1	DAC CH1 volume. -0dB to -127.5dB, 0.5dB steps • 8'd0: 0dB • 8'd255: -127.5dB

Register 75: VOLUME CH2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME_CH2	DAC CH2 volume. -0dB to -127.5dB, 0.5dB steps • 8'd0: 0dB • 8'd255: -127.5dB

Register 81-76: RESERVED

Register 82: DAC VOL UP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Linear step size from the current volume to a target volume, represented as a fraction of full-scale. $\text{vol\_step\_rate [inc/s]} = \frac{\text{DAC\_VOL\_RATE\_UP} \cdot FS}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 83: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Linear step size from the current volume to a target volume, represented as a fraction of full-scale. $\text{vol\_step\_rate [inc/s]} = \frac{\text{DAC\_VOL\_RATE\_DOWN} \cdot FS}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 84: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Linear step size from the current volume to a target volume, represented as a fraction of full-scale. Only used during abnormal mute (PLL unlock or BCK_WS ratio failed) $\text{vol\_step\_rate [inc/s]} = \frac{\text{DAC\_VOL\_RATE\_FAST} \cdot FS}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'hFF: Fastest change (default)

Register 85: RESERVED

Register 86: DAC MUTE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	DAC_MUTE_CH2	• 1'b0: Normal CH2 operation (default) • 1'b1: Mute CH2
[0]	DAC_MUTE_CH1	• 1'b0: Normal CH1 operation (default) • 1'b1: Mute CH1

Register 87: DAC INVERT

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	DAC_INVERT_CH2	Invert the output on CH2 at the input to the noise shaped modulator (NSMOD). • 1'b0: Uninverted CH2 DAC output (default) • 1'b1: Inverted CH2 DAC output
[0]	DAC_INVERT_CH1	Invert the output on CH1 at the input to the noise shaped modulator (NSMOD). • 1'b0: Uninverted CH1 DAC output (default) • 1'b1: Inverted CH1 DAC output

Register 88: FILTER SHAPE

Bits	[7:3]	[2:0]
Default	5'b10111	3'd0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 89: IIR BANDWIDTH & S/PDIF SEL

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'd4

Bits	Mnemonic	Description
[7:4]	SPDIF_SEL	Selects the S/PDIF data input pin. • 4'd0: Disconnected • 4'd1: DATA1 • 4'd2: DATA2 • 4'd3: GPIO1 • 4'd4: GPIO2 • 4'd5: GPIO3 • 4'd6: GPIO4 • 4'd7: GPIO5 • 4'd8: GPIO6 • 4'd9: GPIO7 • 4'd10: GPIO8 • Others: Reserved Note: GPIOx pins also require the GPIOx_SDB to be enabled.
[3]	VOLUME_HOLD	Hold volume coefficients to allow for all channels to update at same time. • 1'b0: Channel volume will update with changes to reg 74-75. • 1'b1: Channel volumes will not update.
[2:0]	IIR_BW	Controls the IIR bandwidth in the digital datapath. • 3'd0: Reserved • 3'd1: BW * 8 • 3'd2: BW * 4 • 3'd3: BW * 2 • 3'd4: BW (default) • 3'd5: BW / 2 • 3'd6: BW / 4 • 3'd7: BW / 8

Register 90: DAC PATH CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	BYPASS_IIR	Bypass the IIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[1]	BYPASS_FIR4X	Bypass the 4X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[0]	BYPASS_FIR2X	Bypass the 2X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed

Register 94-91: THD C2

Bits	[31:16]	[15:0]
Default	16'd0	16'd0

Bits	Mnemonic	Description
[31:16]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 106-95: RESERVED

Register 110-107: THD C3

Bits	[31:16]	[15:0]
Default	16'd0	16'd0

Bits	Mnemonic	Description
[31:16]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 122-111: RESERVED

Register 123: AUTOMUTE ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd63	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_EN_CH2	• 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default)
[0]	AUTOMUTE_EN_CH1	• 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default)

Register 125-124: AUTOMUTE TIME

Bits	[15:12]	[11]	[10:0]
Default	4'b0000	1'b1	11'h0F

Bits	Mnemonic	Description
[15:12]	RESERVED	N/A
[11]	MUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $\text{Time [s]} = \frac{2^{18}}{\text{AUTOMUTE\_TIME} \cdot FS}$

Register 127-126: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. Shift right 1 bit corresponds to -6dB. • 16'h0001: -132dB • 16'h0008: -119dB (default) • 16'hFFFF: -42dB Note: Only applies to PCM automute conditions.

Register 129-128: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. Shift right 1 bit corresponds to -6dB. • 16'h0001: -132dB • 16'h000A: -117.5dB (default) • 16'hFFFF: -42dB Note: Only applies to PCM automute conditions.

Register 130: SOFT RAMP CONFIG

Bits	[7:5]	[4:0]
Default	3'b000	5'd3

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $\text{Time [s]} = 4096 \cdot \frac{2^{\text{SOFT\_RAMP\_TIME}+1}}{\text{CLK\_IDAC[Hz]}}$

Register 134-131: RESERVED

Register 135: PROGRAM RAM CONTROL

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'b00000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SPDIF_LOAD_USER_BITS	Selects whether the S/PDIF Channel Status or User Data bits are available to readback from the register interface. Subframes A and B must have the same user data bits for readback. • 1'b0: Channel Status bits on the register interface (default) • 1'b1: User Data bits on the register interface
[6:2]	RESERVED	N/A
[1]	PROG_COEFF_WE	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default). • 1'b1: Enables write signal to the coefficient RAM.
[0]	PROG_COEFF_EN	Enables the custom oversampling filter coefficients. • 1'b0: Uses a built-in filter selected by filter_shape (default). • 1'b1: Uses the coefficients programmed via prog_coeff_data.

Register 136: S/PDIF READ CONTROL

Bits	[7:5]	[4:0]
Default	3'b000	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	SPDIF_DATA_SEL	Selects the byte of the S/PDIF payload in register 251 spdif_payload_read • 24 bytes total

Register 137: PROGRAM RAM ADDRESS

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects the 2x stage of the oversampling filter (default). • 1'b1: Selects the 4x stage of the oversampling filter.
[6:0]	PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register 140-138: PROGRAM RAM DATA

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_IN	A 24-bit signed filter coefficient that will be written to the address defined in prog_coeff_addr.

Register 145-141: RESERVED

Readback Registers

Register 224: RESERVED

Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h63

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID. • ES9039Q2M: 0x63

Register 228-226: RESERVED

Register 230-229: INTERRUPT STATES

Bits	[15:14]	[13:12]	[11]	[10:8]	[7]	[6]	[5:4]	[3:2]	[1:0]
Default		-	-		-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:12]	INPUT_SELECT_OVERRIDE_STATE	State of the INPUT_SELECT_OVERRIDE interrupt. Note: Interrupt clear bits are required to reset value.
[11]	TDM_DATA_VALID_STATE	State of the TDM_DATA_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[10:8]	RESERVED	N/A
[7]	BCK_WS_FAIL_STATE	State of the BCK_WS_FAIL interrupt. Note: Interrupt clear bit is required to reset value.
[6]	DOP_VALID_STATE	State of the DOP_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[5:4]	SS_FULL_RAMP_STATE	State of each channel's SS_FULL_RAMP interrupt. Note: Interrupt clear bit is required to reset value.
[3:2]	AUTOMUTE_STATE	State of each channel's AUTOMUTE_STATE interrupt. Note: Interrupt clear bit is required to reset value.
[1:0]	VOL_MIN_STATE	State of each channel's VOL_MIN_STATE interrupt. Note: Interrupt clear bit is required to reset value.

Register 233-231: RESERVED

Register 235-234: INTERRUPT SOURCES

Bits	[15:14]	[13:12]	[11]	[10:8]	[7]	[6]	[5:4]	[3:2]	[1:0]
Default		-	-		-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:12]	INPUT_SELECT_OVERRIDE_SOURCE	Output of the AUTO_INPUT_SELECT logic.
[11]	TDM_DATA_VALID_SOURCE	TDM data valid flag.
[10:8]	RESERVED	N/A
[7]	BCK_WS_FAIL_SOURCE	Validity of BCK, WS, and ASYNC_LOCK flag. Requires respective monitor bits to be set.
[6]	DOP_VALID_SOURCE	Valid DoP flag for Channels 1 and 2.
[5:4]	SS_FULL_RAMP_SOURCE	Channel flag for whether it is automute is active.
[3:2]	AUTOMUTE_SOURCE	Channel flag for whether it is automute is active.
[1:0]	VOL_MIN_SOURCE	Channel flag for whether the corresponding volume register = 0x00

Register 239-236: RESERVED

Register 240: GPIO READBACK

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	GPIO8_I_READ	GPIO8 input readback.
[6]	GPIO7_I_READ	GPIO7 input readback.
[5]	GPIO6_I_READ	GPIO6 input readback.
[4]	GPIO5_I_READ	GPIO5 input readback.
[3]	GPIO4_I_READ	GPIO4 input readback.
[2]	GPIO3_I_READ	GPIO3 input readback.
[1]	GPIO2_I_READ	GPIO2 input readback.
[0]	GPIO1_I_READ	GPIO1 input readback.

Register 241: VOL MIN READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	VOL_MIN_CH2	Volume min flag ch2
[0]	VOL_MIN_CH1	Volume min flag ch1

Register 242: AUTOMUTE READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_CH2	Automute status ch2
[0]	AUTOMUTE_CH1	Automute status ch1

Register 243: SOFT RAMP UP READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	SS_RAMP_UP_CH2	Soft ramped up flag ch2
[0]	SS_RAMP_UP_CH1	Soft ramped up flag ch1

Register 244: SOFT RAMP DOWN READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	SS_RAMP_DOWN_CH2	Soft ramped down flag ch2
[0]	SS_RAMP_DOWN_CH1	Soft ramped down flag ch1

Register 245: INPUT STREAM READBACK

Bits	[7:5]	[4]	[3]	[2]	[1:0]
Default		-	-	-	-

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	SPDIF_VALID	S/PDIF valid flag
[3]	TDM_DATA_VALID	TDM valid data flag
[2]	DOP_VALID	DoP valid flag
[1:0]	INPUT_SELECT_OVERRIDE	AUTO_INPUT_SEL value • 2'd0: PCM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: S/PDIF

Register 248-246: PROG COEFF OUT READ

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_OUT	Programmable FIR coefficient readback

Register 250-249: RESERVED

Register 251: S/PDIF DATA READ

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPDIF_DATA_READ	Contains a byte of the S/PDIF payload. Controlled by register 136[4:0] spdif_data_sel

ES9039Q2M Reference Schematics

Typical Application Schematic

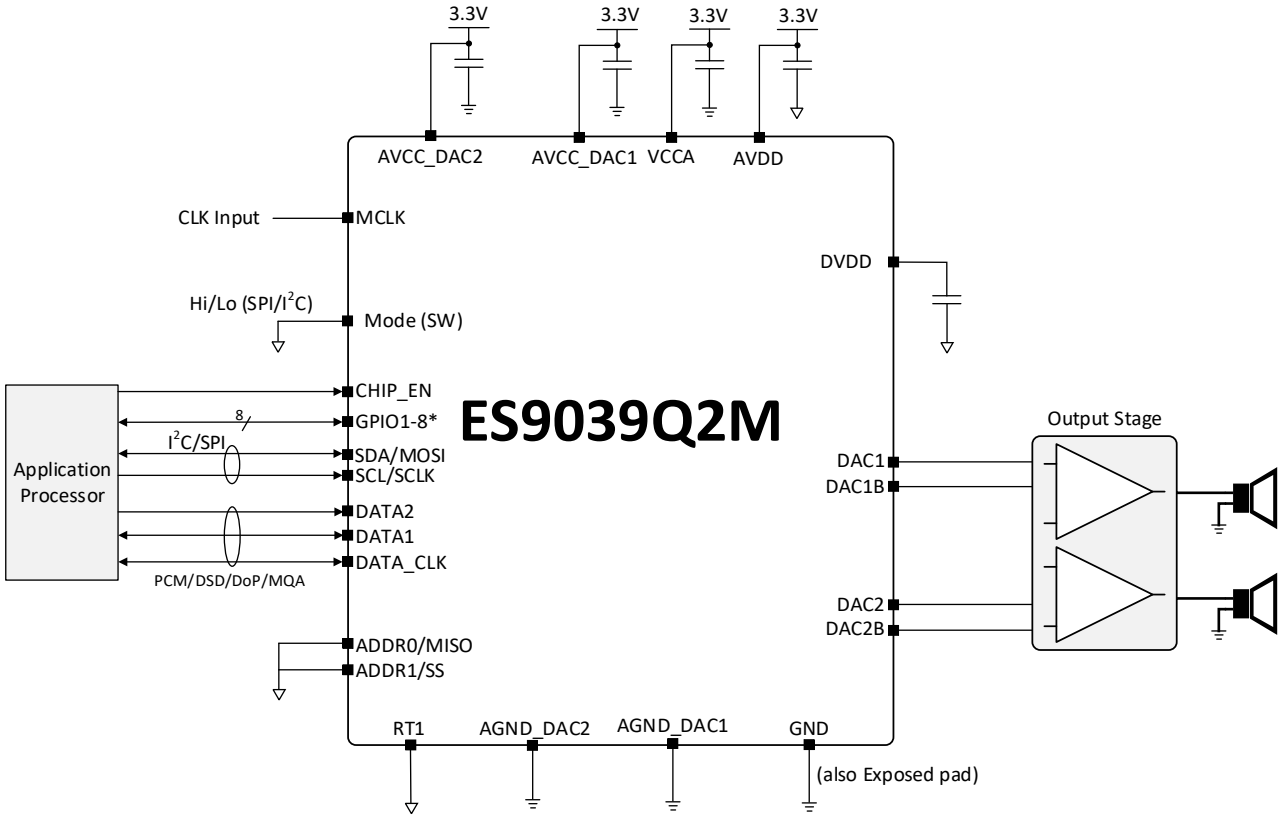


Figure 24 - Typical ES9039Q2M Software Mode Application Diagram

Note: See GPIO section for configuration of GPIOs including GPIO8.

Hardware (HW) Mode

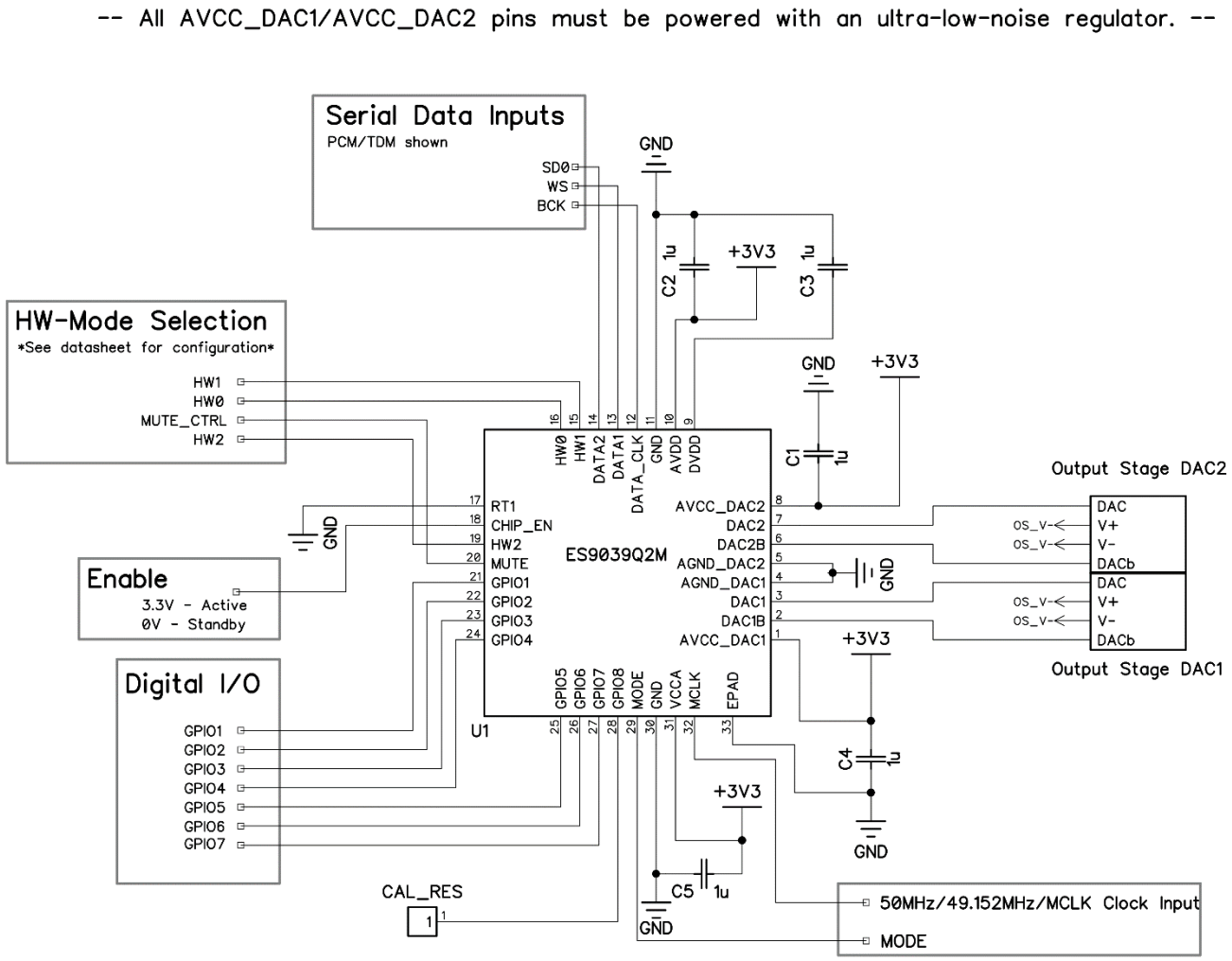


Figure 25 - Hardware (HW) Mode Reference Schematic for ES9039Q2M

Note: ES9039Q2M has an exposed pad (EPAD, Pin 33) and should be connected to ground.

Software (SW) Mode

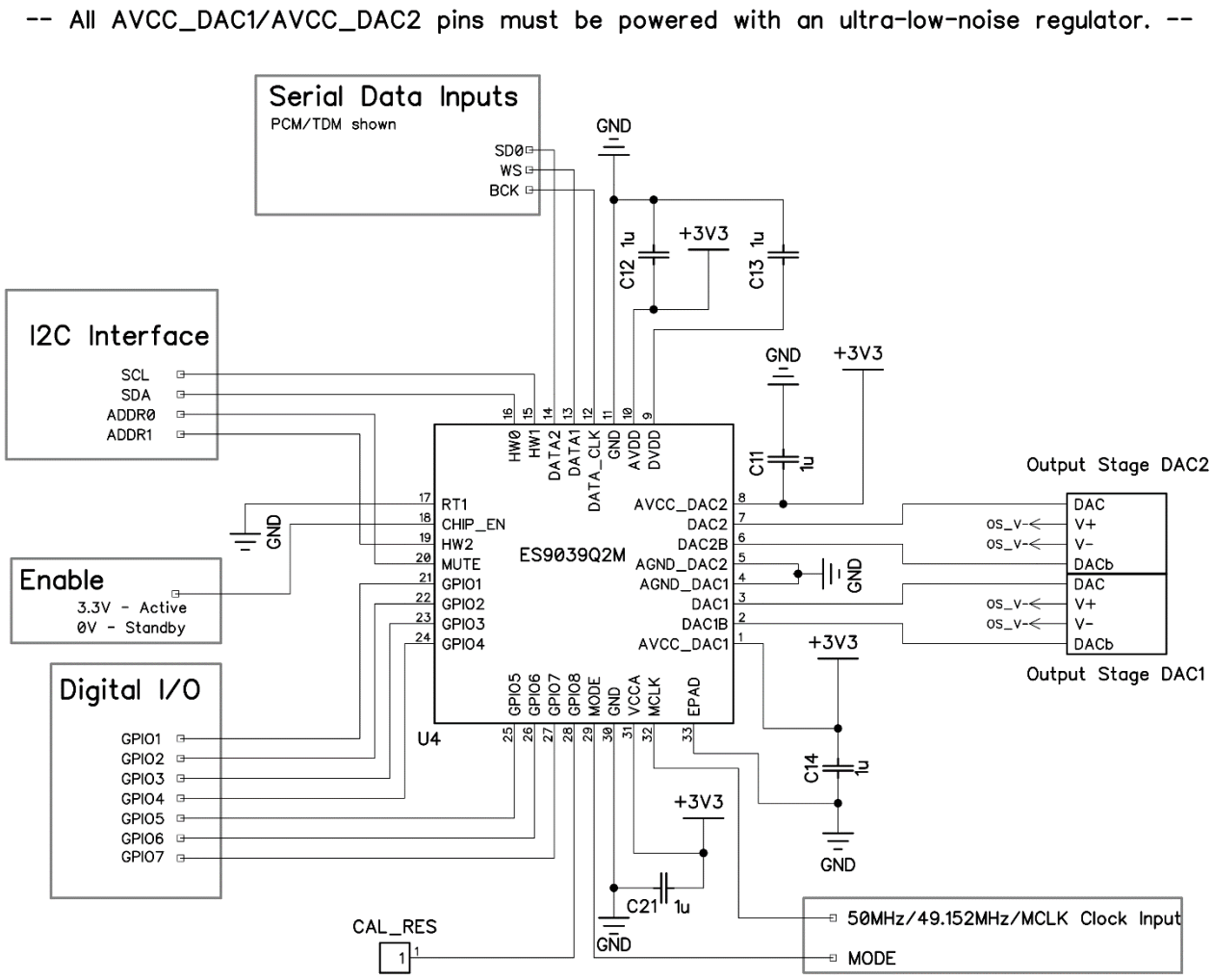


Figure 26 - Software Mode Reference Schematic for ES9039Q2M

Note: ES9039Q2M has an exposed pad (EPAD, Pin 33) and should be connected to ground.

Recommended Output Stage

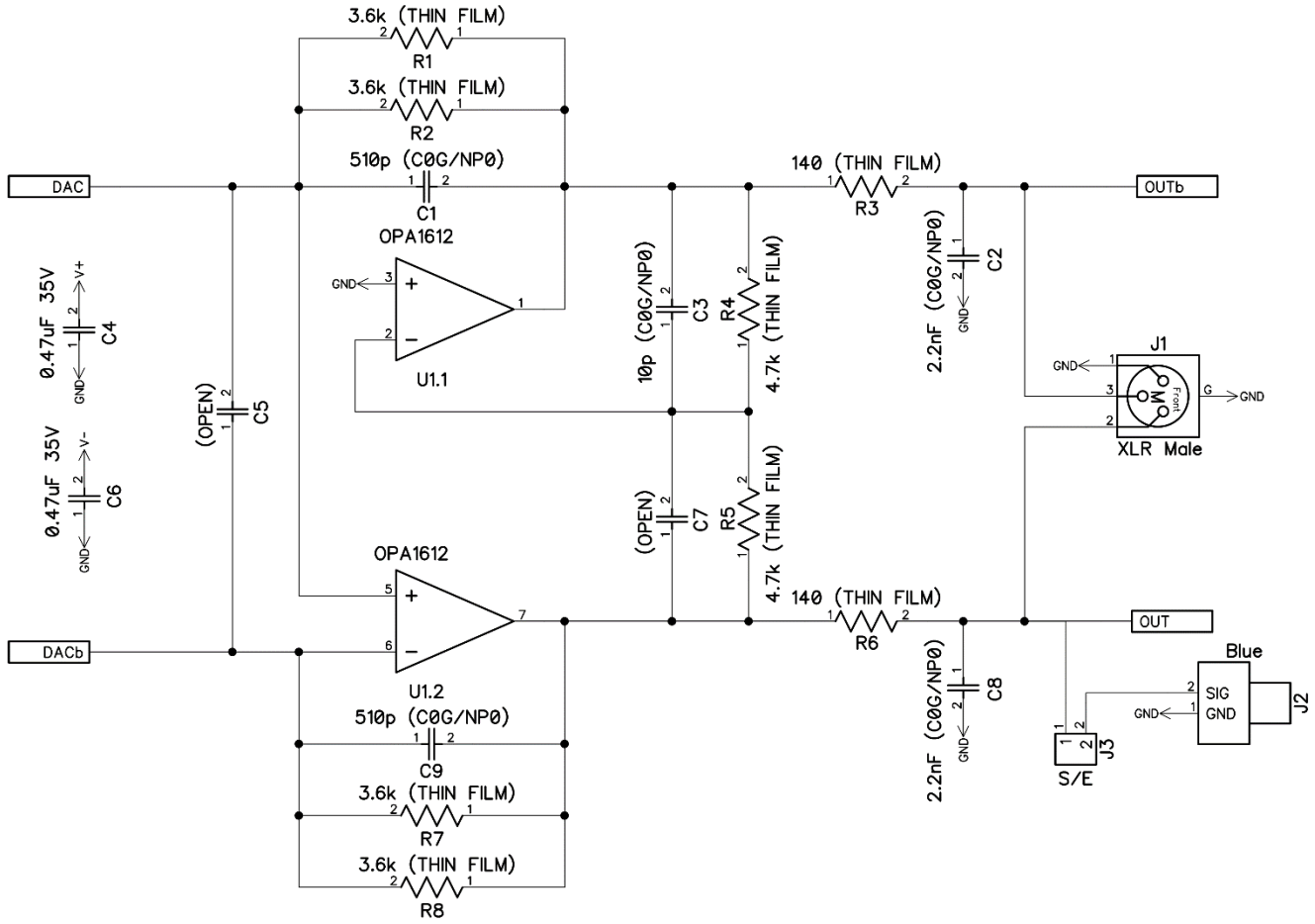


Figure 27 - Output Stage Schematic for ES9039Q2M

Note 1: Schematic is representative of ES9039Q2M EVB v2.1
Note 2: A 3 op-amp output stage schematic with slightly improved THD+N performance with a slight increase in noise is available, see distributor or FAE for more information if required.
Note 3: C1, C3 & C9 values are chosen specifically for OPA1612, change depending on desired frequency response.

Recommended Power Supply

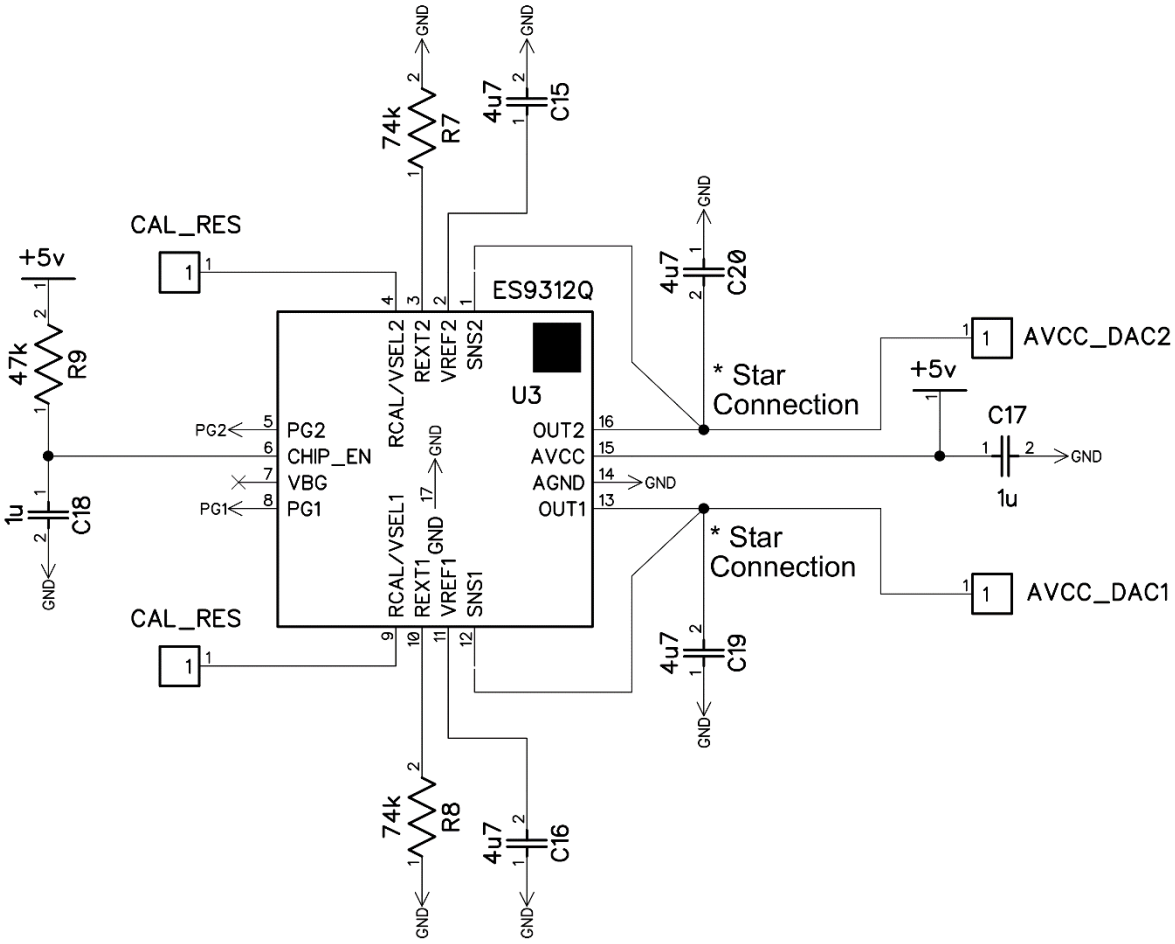
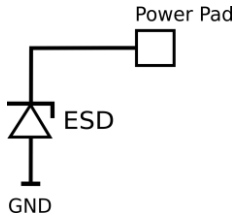
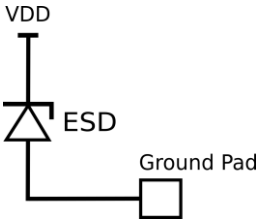
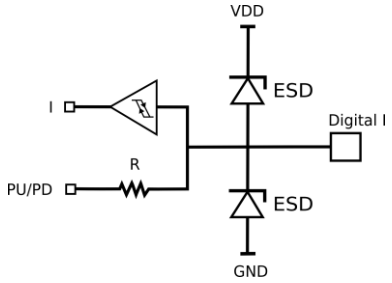
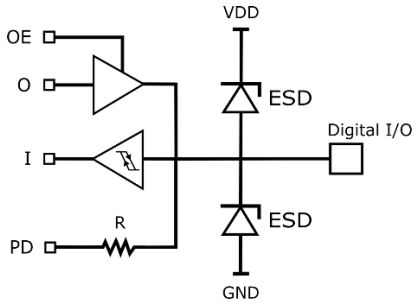


Figure 28 - ES9039Q2M Power Supply Schematic

Note: In all configurations V_{BG} must remain floating. VSENSEx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

Internal Pad Circuitry

Pin Name	Type	Pin	Equivalent Circuit
AVCC_DAC1 AVCC_DAC2 AVDD VCCA	Power	1 8 10 31	
AGND_DAC1 AGND_DAC2 GND GND	Ground	4 5 11 30	
CHIP_EN	Reset	18	
DATA_CLK DATA1 DATA2 SCLK/SCL/HW1 MOSI/SDA/HW0 RT1 SS/ADDR1/HW2 MISO/ADDR0/MUTE_CTRL GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 MODE	Digital I/O	12 13 14 15 16 17 19 20 21 22 23 24 25 26 27 29	

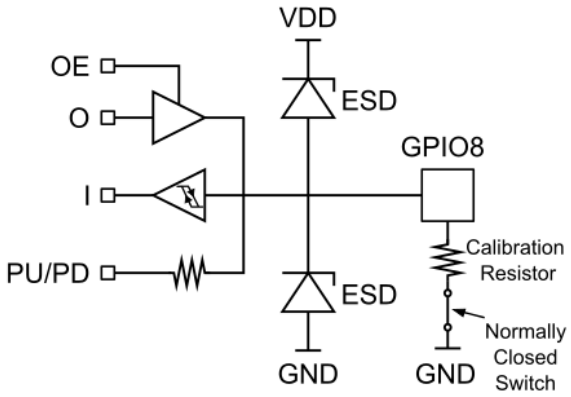
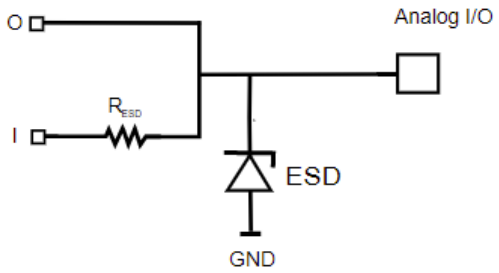
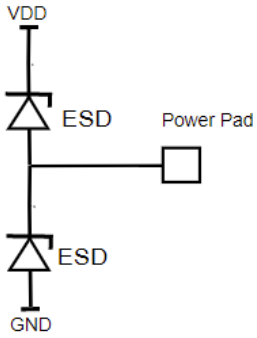
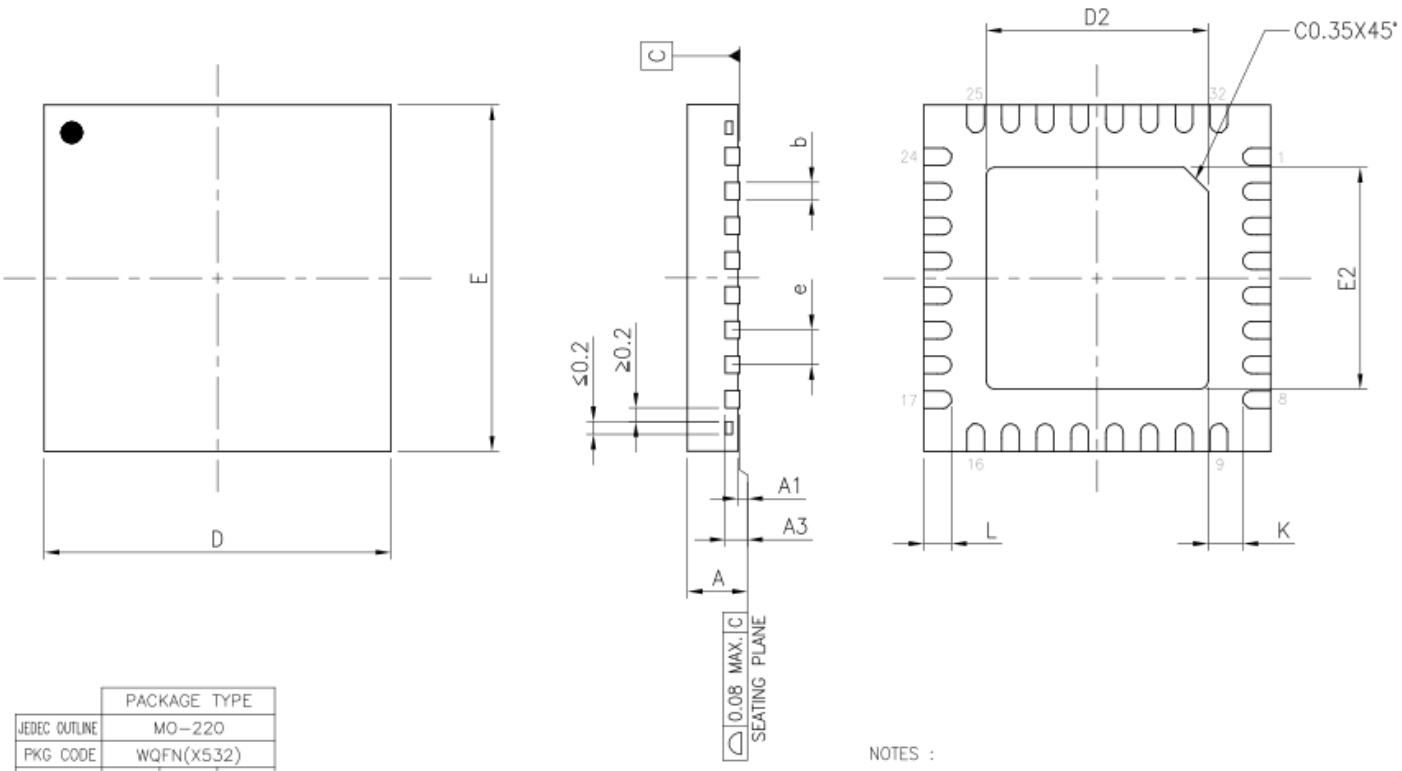
GPIO 8	Digital I/O Cal_Res	28	
DAC1B DAC1 DAC2B DAC2 MCLK	Analog IO DAC	2 3 6 7 32	
DVDD	IO Power	9	

Table 33 - Internal Pad Circuitry

32 QFN Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X532)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
134X13* MIL	3.15	3.20	3.25	3.15	3.20	3.25	V	V	W(V)HHD-2

""表示此用字元,此处用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 29 - ES9039Q2M 32 QFN Package Dimensions

32 QFN Top View Marking

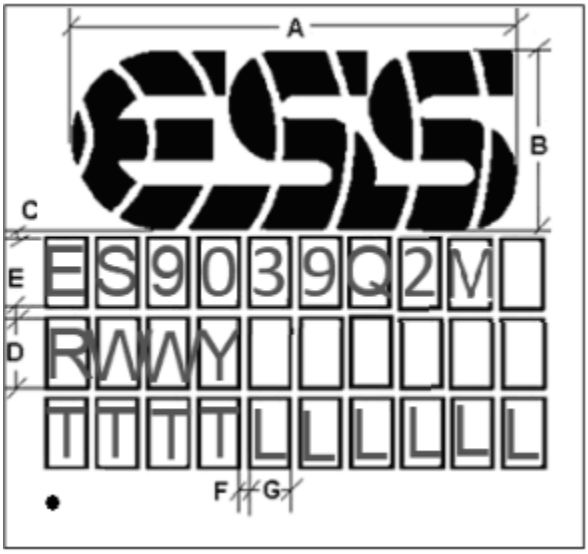


Figure 30 - ES9039Q2M Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
32 QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	Tracking Number
W	Work Week
Y	Last Digit of Year
L	Low Number
R	Silicon Revision

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

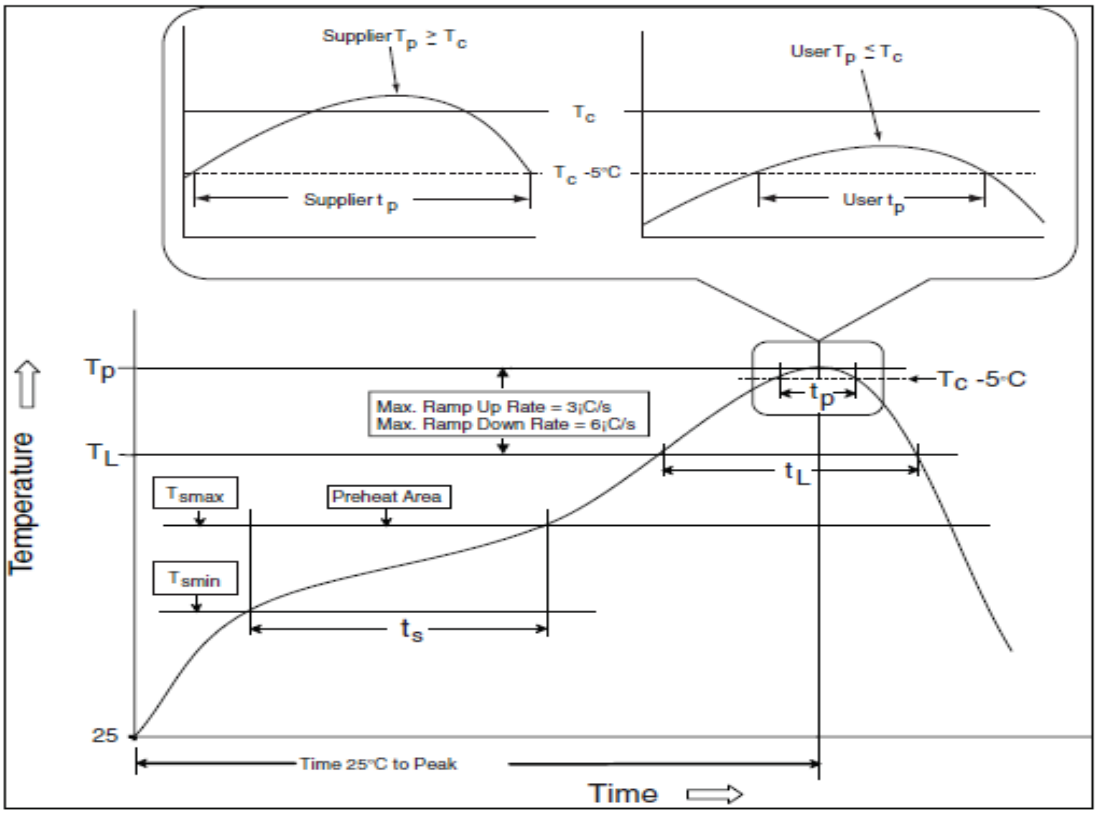


Figure 31 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 34 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2-Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 35 - RPC-2 Pb Free Classification Temperature

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9039Q2M	SABRE 32-bit High Performance 2 Channel DAC	5mm x 5mm 32 QFN

Table 36 - Ordering Information

Revision History

Current Version 0.2

Rev.	Date	Notes
0.1.2	March, 2023	Initial release
0.2	September,2024	• Updated formatting • Updated PCM Digital Filters with 64FS Mode Filter • Updated 32 QFN Package Dimensions clarity • Updated Calibration Resistor section • Updated Reference Schematic power supplies and output stage • Updated reference to MCLK & SYS_CLK for clock gearing for clarity • Updated register description Reg5[5:4,2], 42[6, 4, 3], 48-56, 57[0], 62[4, 3], 64[4:0], 65[4:0],123[1,0] • Unreserved Reg 60[5] TDM_DAISY_CHAIN • Unreserved Reg 135[7] SPDIF_LOAD_USER_BITS